SM30 Block Diagram

Project code: 91.4BT01.001
PCB P/N : 48.4BT01.001
Revision : 08239-SA

Crystal 14.318MHz
CLK GEN. ICS 9LPRS929 3
Mobile CPU Penryn 4, 5
SMSC EMC2103 29
HOST BUS 667/800/1066MHz@1.05V
DDR3 800/1033 MHz 12,13
DDR3 800/1033 MHz 12,13
Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
6,7,8,9,10,11
LCD 15
CRT 17
X4 DMI 400MHz
C-Link0
Crystal 32.768KHz
Crystal 25MHz
LAN Giga LAN BCM5764
TXFM
RJ45
Mini Card (Robson2/3G)
Mini Card Kedron a/b/g/n 28 (WLAN)
PCIe
ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
4 SATA
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
18,19,20,21
Int MIC 15
MIC In 32
32 Line Out (SPDIF)
Codec ALC272 30
AZALIA
32 INT.SPKR 1.5W
OP AMP G1454 31
LPC BUS
Crystal 32.768KHz
KBC Winbond WPCE773LA0DG 33
SPI
BIOS (2MB) 34
Launch Buttom 35
LPC DEBUG CONN. 34
Touch Pad 33
INT. KB 33
Daughter Board 08621
Launch Board
SATA
USB
HDD SATA 23
ODD SATA 22
Mini USB Blue Tooth 24
Finger Printer 26
USB 2 Port 25
Camera 15
USB 1 Port
CardReader Realtek RTS5159 27
MS/MS Pro/xD /MMC/SD 5 in 1 27

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC TPS51125 50	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC TPS51124 51	
INPUTS	OUTPUTS
DCBATOUT	1D05V_M(16A) 1D5V_S3(12A)

RT9026 52	
1.5V_S3	DDR_VREF_S3 (1.2A)

G9131 52	
3D3V_S0	2D5V_S0 (300mA)

TPS51117 54	
DCBATOUT	1D8V_S0 (9.4A)

CHARGER BQ24750 55	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC ISL6266A 49	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 38A

GFX DC/DC ISL6263 53	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 0~1.3V 6.5A

SM30

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Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	SM30	SB

Date: Tuesday, October 28, 2008 Sheet 1 of 45

ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

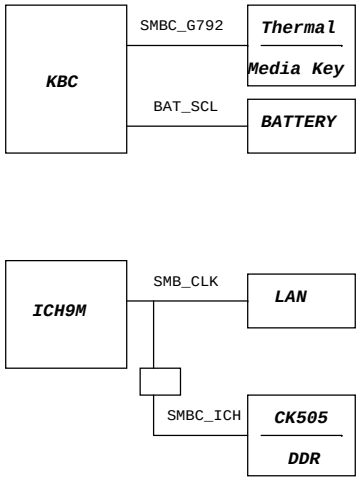
SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

SMBus



USB Table

USB	
Pair	Device
0	USB1(IO board)
1	USB1
2	CAMERA
3	MINIC2(WLAN)
4	NC
5	NC
6	FingerPrint
7	BLUETOOTH
8	NC
9	USB2(HS)
10	MINIC1(IO BOARD)
11	CARD READER

PCIE Routing

LANE1	LAN BCM5764
LANE2	MiniCard WLAN
LANE3	MiniCard(Robson2G/3G)

SM30

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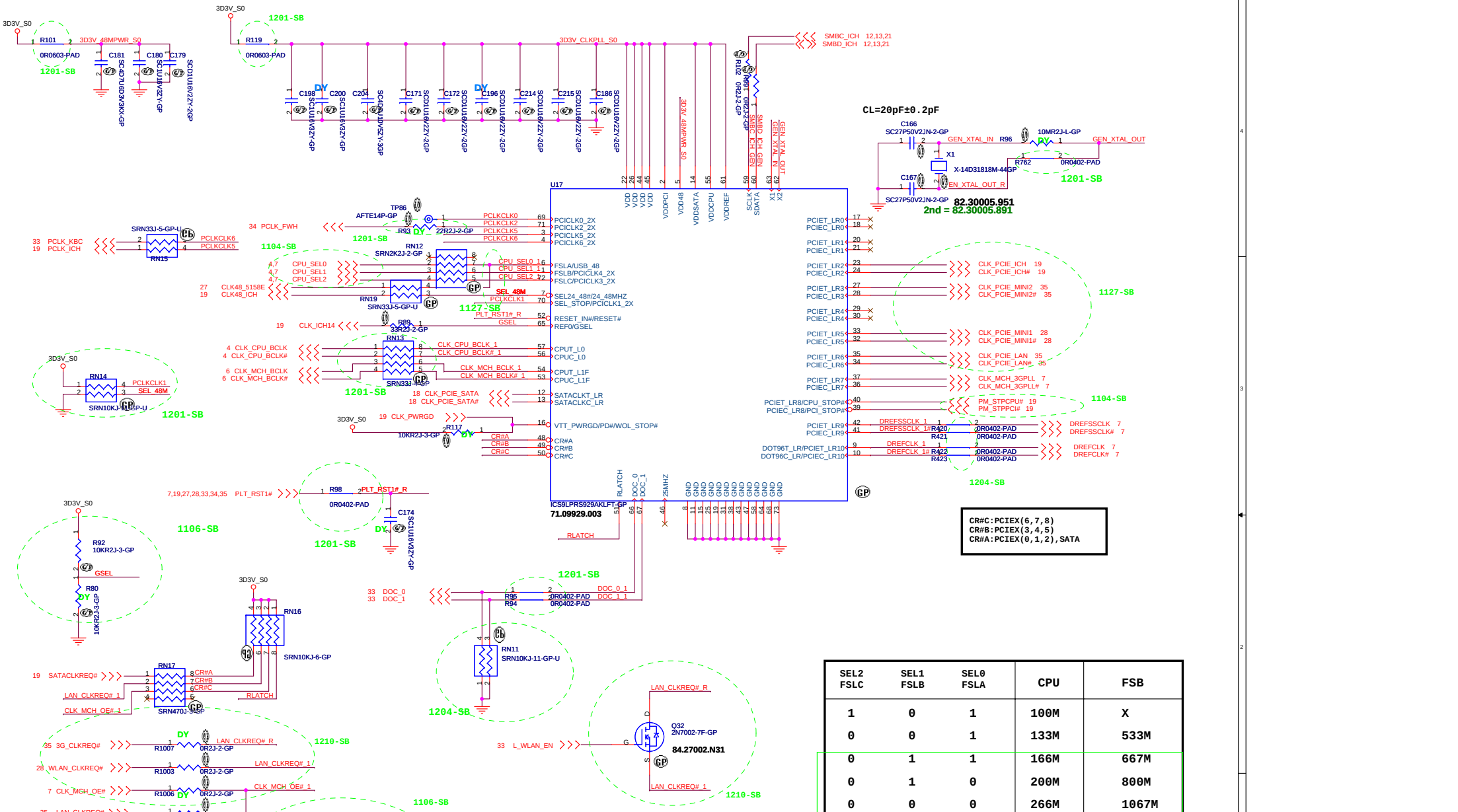
Title: Reference

Size: A3 | Document Number: SM30 | Rev: SB

Date: Thursday, December 04, 2008 | Sheet 2 of 45



SEL2 FSLC	SEL1 FSLB	SEL0 FSLA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

GSEL	DOT Freq
0	100MHZ
1	96MHZ

SEL_STOP	Selects pin 39/40
0	PCIEX outputs
1	PCI_STOP#/CPU_STOP#

SEL24_48#/24_48MHZ	OUTPUT
0	48MHZ
1	24MHZ

DOC_0	Real Time Frequency
0	Normal
1	Frequency will transition to a preprogrammed value in the I2C

DOC_1	Real Time Frequency
0	Normal
1	Frequency will transition to a preprogrammed value in the I2C

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Title: Clock Generator

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	SM30	SB

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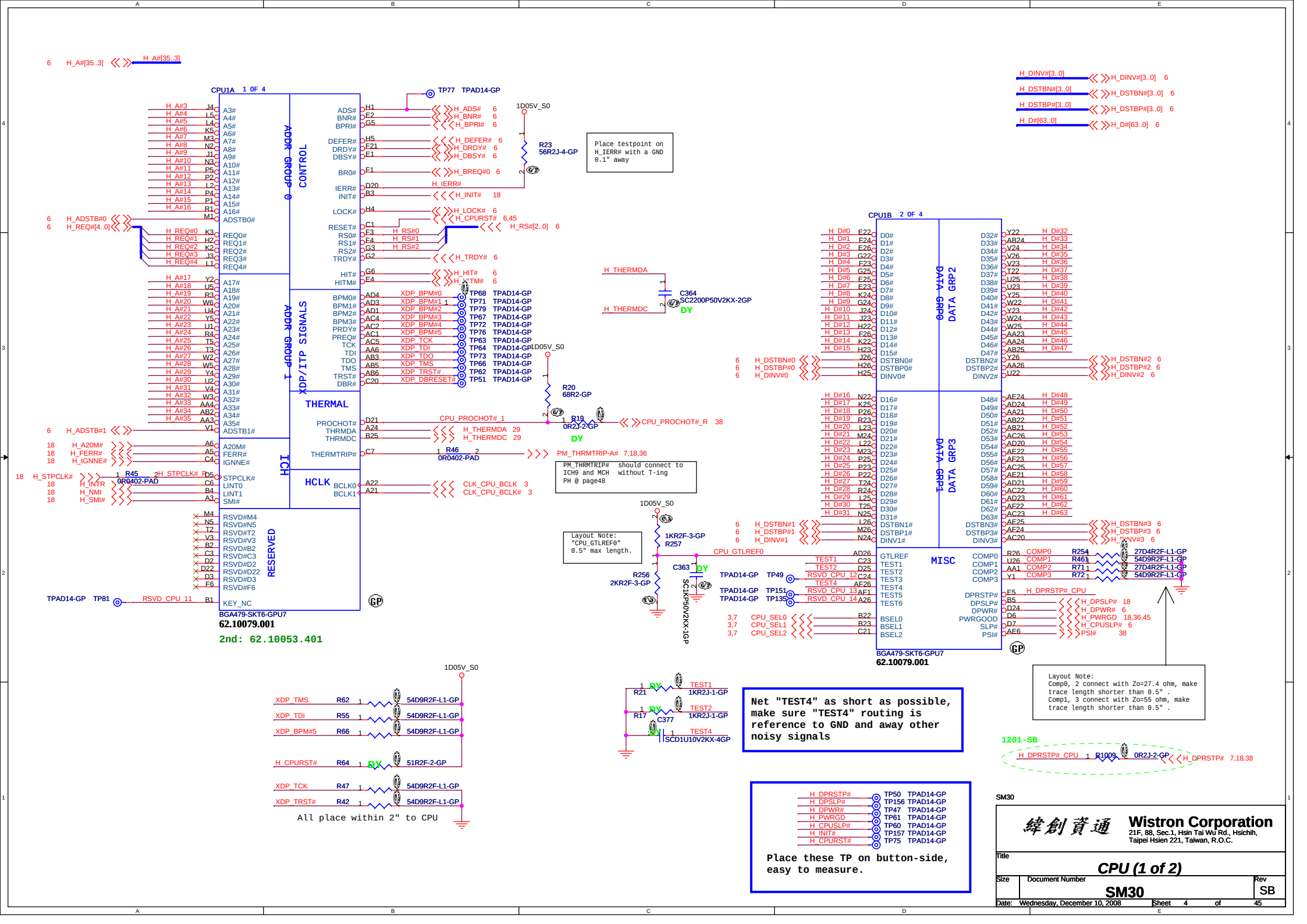
CPU1A 1 0F 4
BGA479-SKT6-GPU7
62.10079.001
2nd: 62.10053.401
CPU1B 2 0F 4
BGA479-SKT6-GPU7
62.10079.001
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
DATA GRP2
DATA GRP3
MISC
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing PH @ page48
Layout Note: "CPU_GTLREF0" 0.5" max length.
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
All place within 2" to CPU
Place these TP on button-side, easy to measure.
1201-SB
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CPU (1 of 2)
SM30
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Wednesday, December 10, 2008
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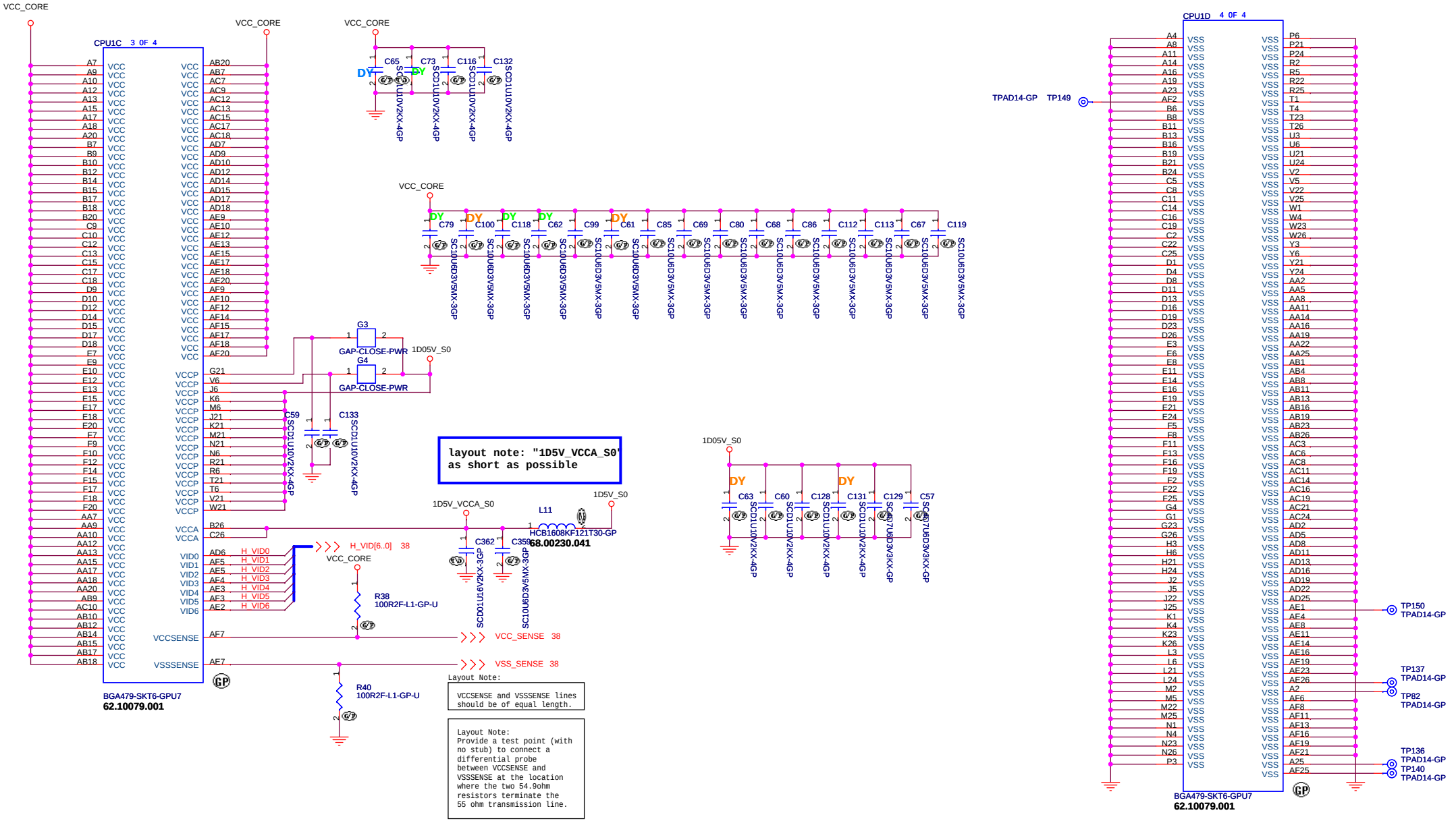

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Title	CPU (2 of 2)
Size	
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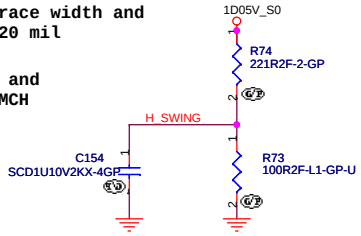
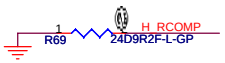
H_SWING routing Trace width and Spacing use 10 / 20 mil

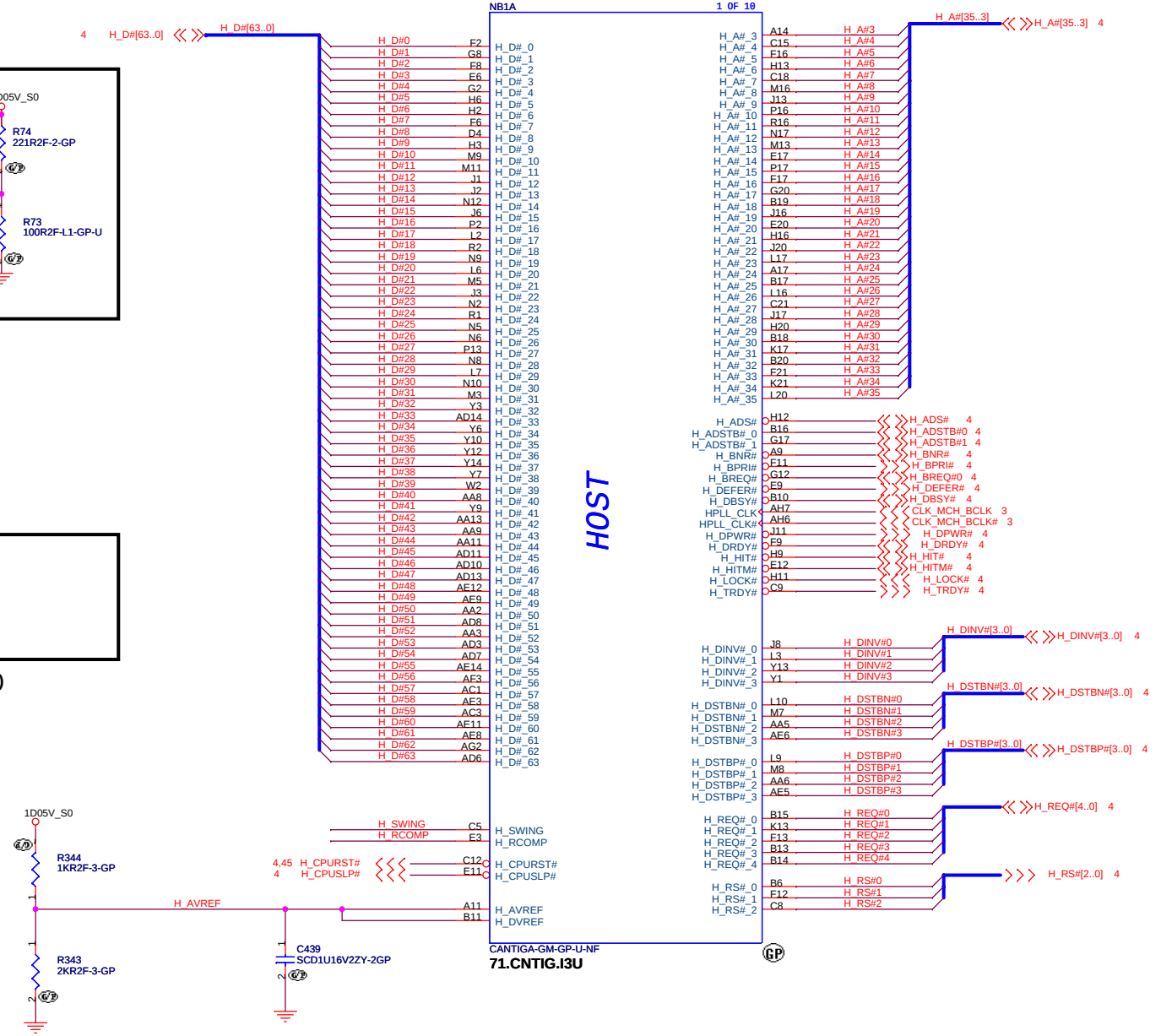
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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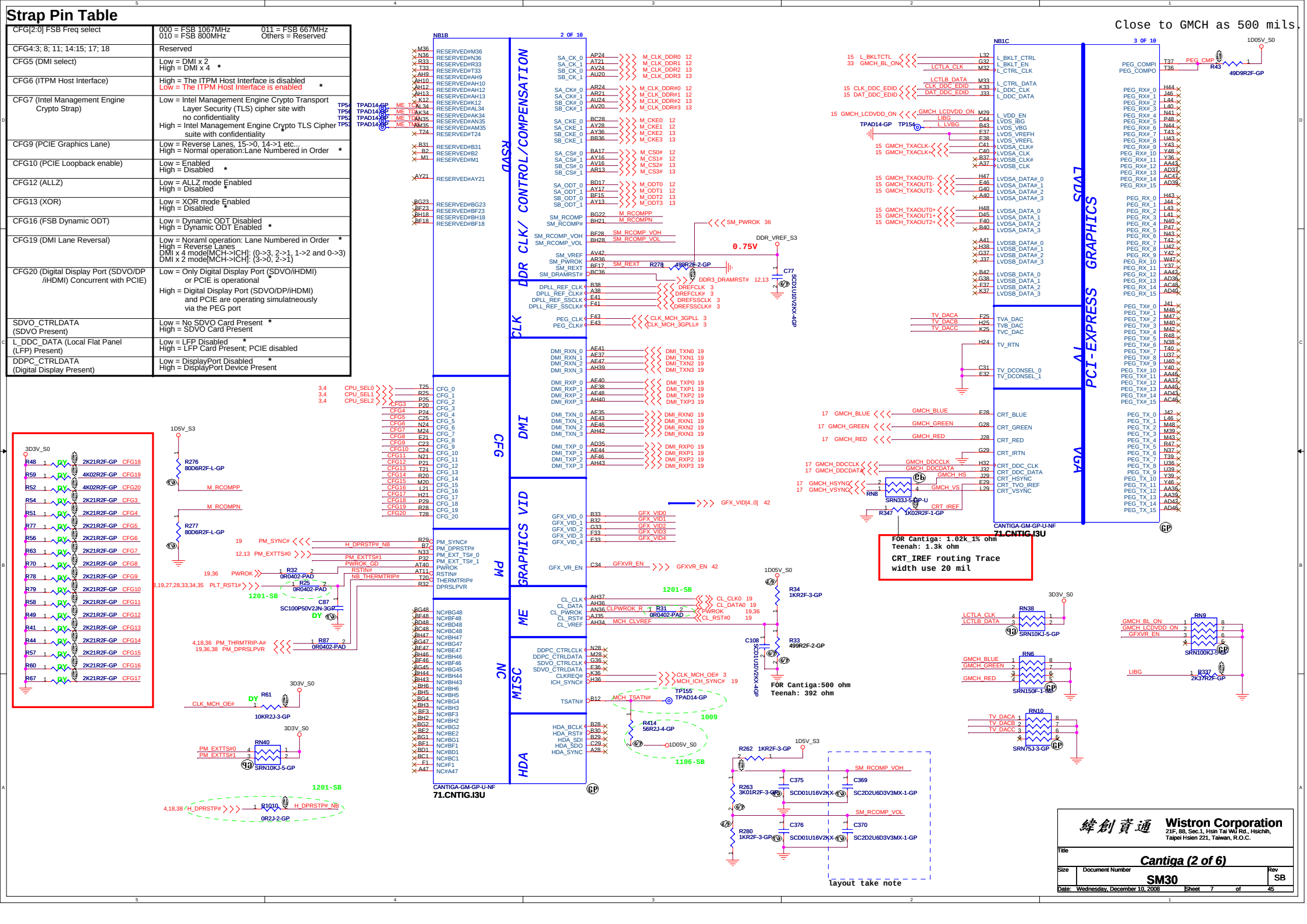
Title	***Cantiga (1 of 6)***
Size	Document Number: **SM30** Rev: SB
Date: Wednesday, December 10, 2008	Sheet 6 of 45

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1067MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG4:3; 8; 11; 14:15; 17; 18	Reserved
CFG5 (DMI select)	Low = DMI x 2 High = DMI x 4 *
CFG6 (ITPM Host Interface)	High = The ITPM Host Interface is disabled Low = The ITPM Host Interface is enabled *
CFG7 (Intel Management Engine Crypto Strap)	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher site with no confidentiality High = Intel Management Engine Crypto TLS Cipher suite with confidentiality *
CFG9 (PCIE Graphics Lane)	Low = Reverse Lanes, 15->0, 14->1 etc... High = Normal operation:Lane Numbered in Order *
CFG10 (PCIE Loopback enable)	Low = Enabled High = Disabled *
CFG12 (ALLZ)	Low = ALLZ mode Enabled High = Disabled *
CFG13 (XOR)	Low = XOR mode Enabled High = Disabled *
CFG16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enabled *
CFG19 (DMI Lane Reversal)	Low = Noraml operation: Lane Numbered in Order * High = Reverse Lanes DMI x 4 mode[MCH->ICH]: (0->3, 2->1, 1->2 and 0->3) DMI x 2 mode[MCH->ICH]: (3->0, 2->1)
CFG20 (Digital Display Port (SDVO/DP /iHDMI) Concurrent with PCIE)	Low = Only Digital Display Port (SDVO/iHDMI) or PCIE is operational * High = Digital Display Port (SDVO/DP/iHDMI) and PCIE are operating simulatneously via the PEG port
SDVO_CTRLDATA (SDVO Present)	Low = No SDVO Card Present * High = SDVO Card Present
L_DDC_DATA (Local Flat Panel (LFP) Present)	Low = LFP Disabled * High = LFP Card Present; PCIE disabled
DDPC_CTRLDATA (Digital Display Present)	Low = DisplayPort Disabled * High = DisplayPort Device Present

Close to GMCH as 500 mils.



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Title: Cantiga (2 of 6)	
Size:	Document Number: SM30
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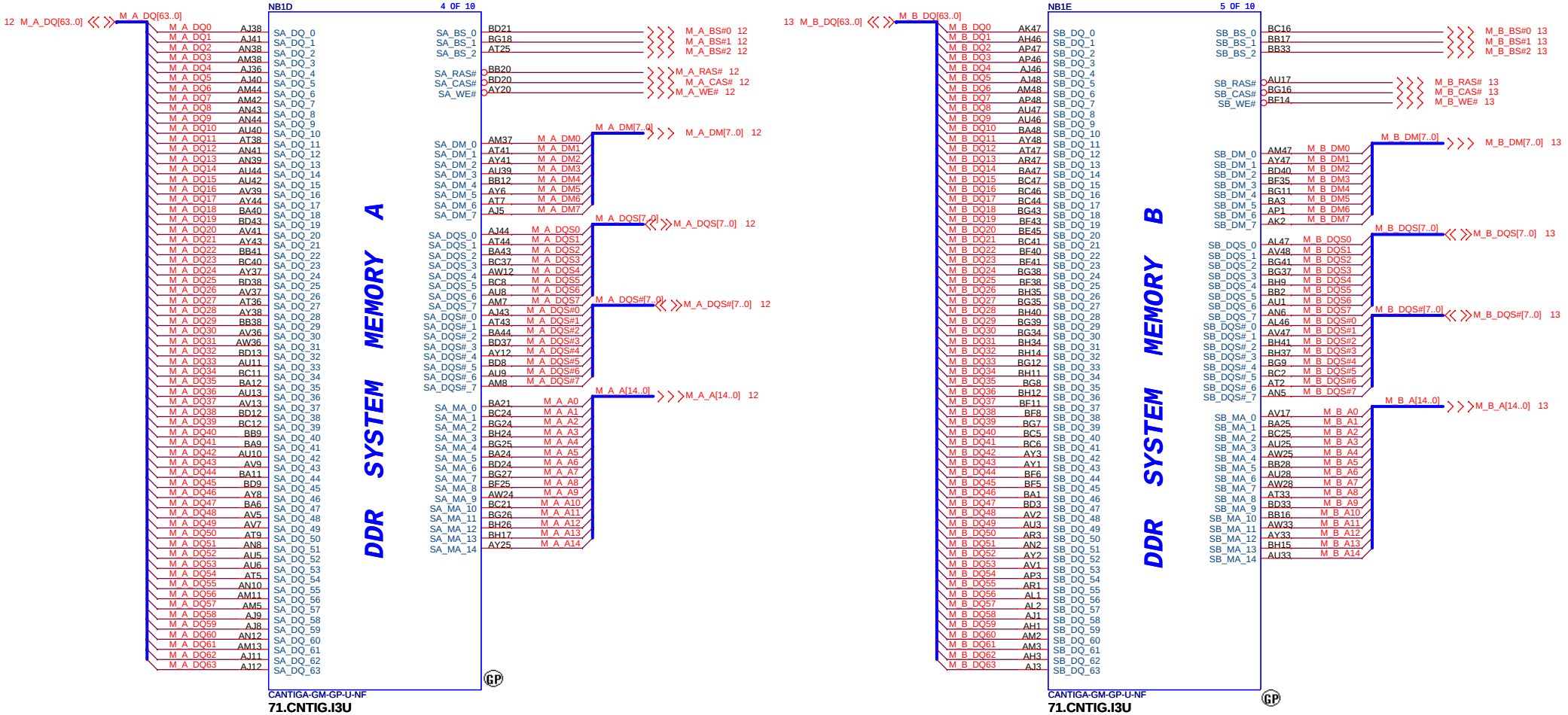

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Title: Cantiga (3 of 6)

Size | Document Number: SM30 | Rev: SB

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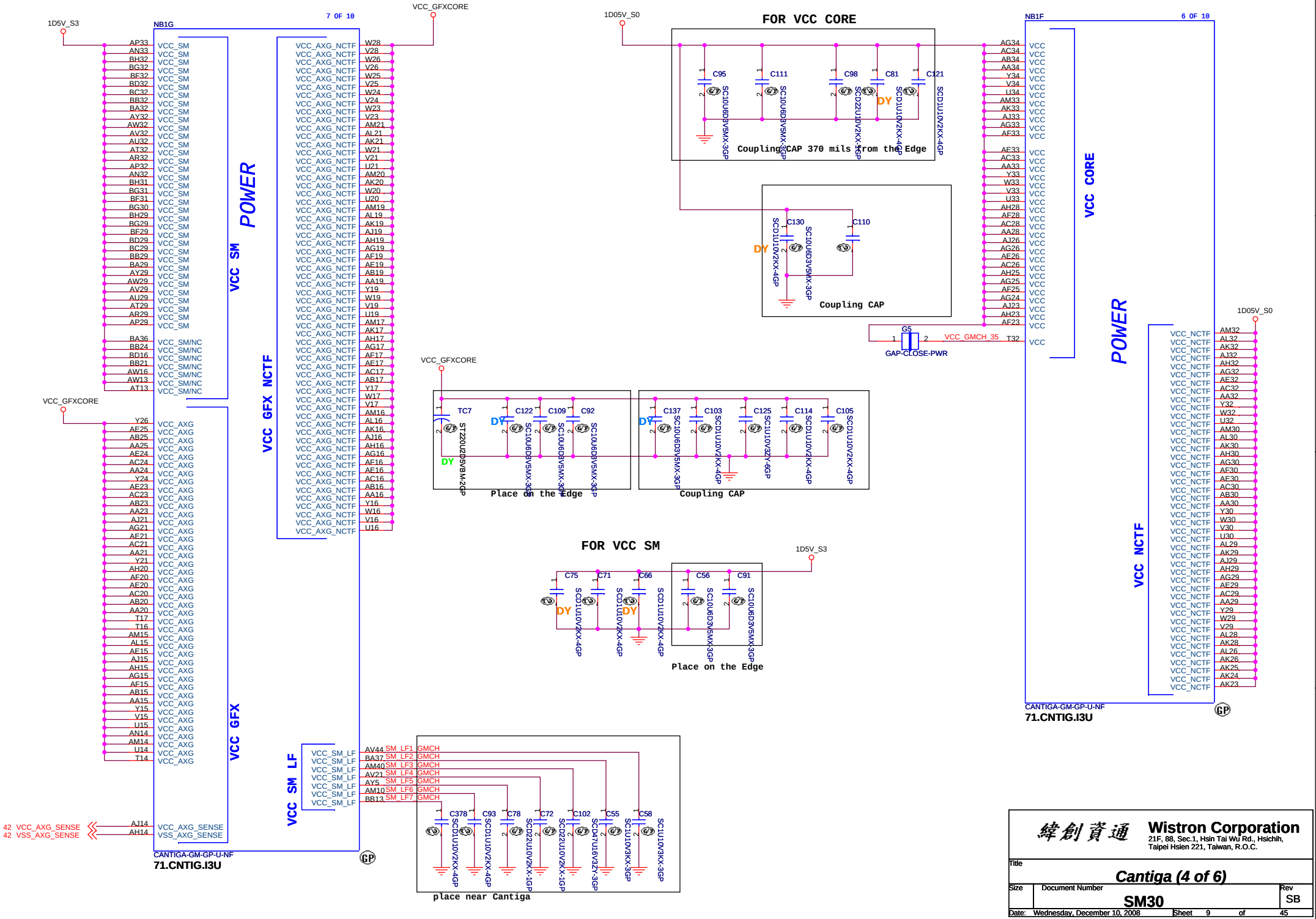

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Title: Cantiga (4 of 6)		
Size	Document Number: SM30	Rev: SB
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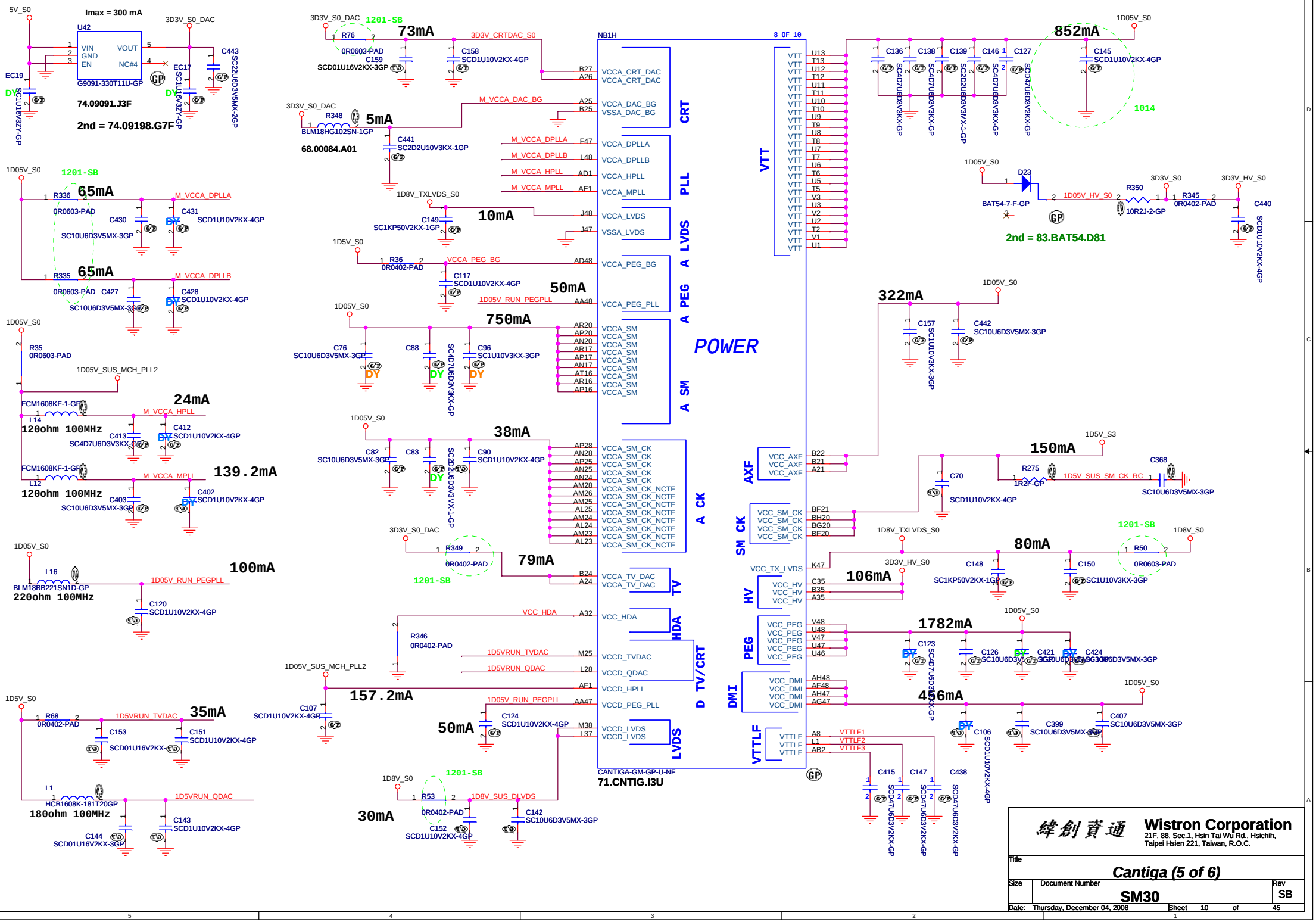
POWER
CANTIGA-GM-GP-U-NF
71.CNTIG.I3U
NB1H
8 OF 10
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
Imax = 300 mA
74.09091.J3F
2nd = 74.09198.G7F
68.00084.A01
2nd = 83.BAT54.D81
1201-SB
73mA
5mA
10mA
50mA
750mA
38mA
79mA
30mA
65mA
65mA
24mA
139.2mA
100mA
35mA
157.2mA
322mA
150mA
80mA
106mA
1782mA
456mA
852mA
1014
120ohm 100MHz
220ohm 100MHz
180ohm 100MHz
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SM30
Rev SB
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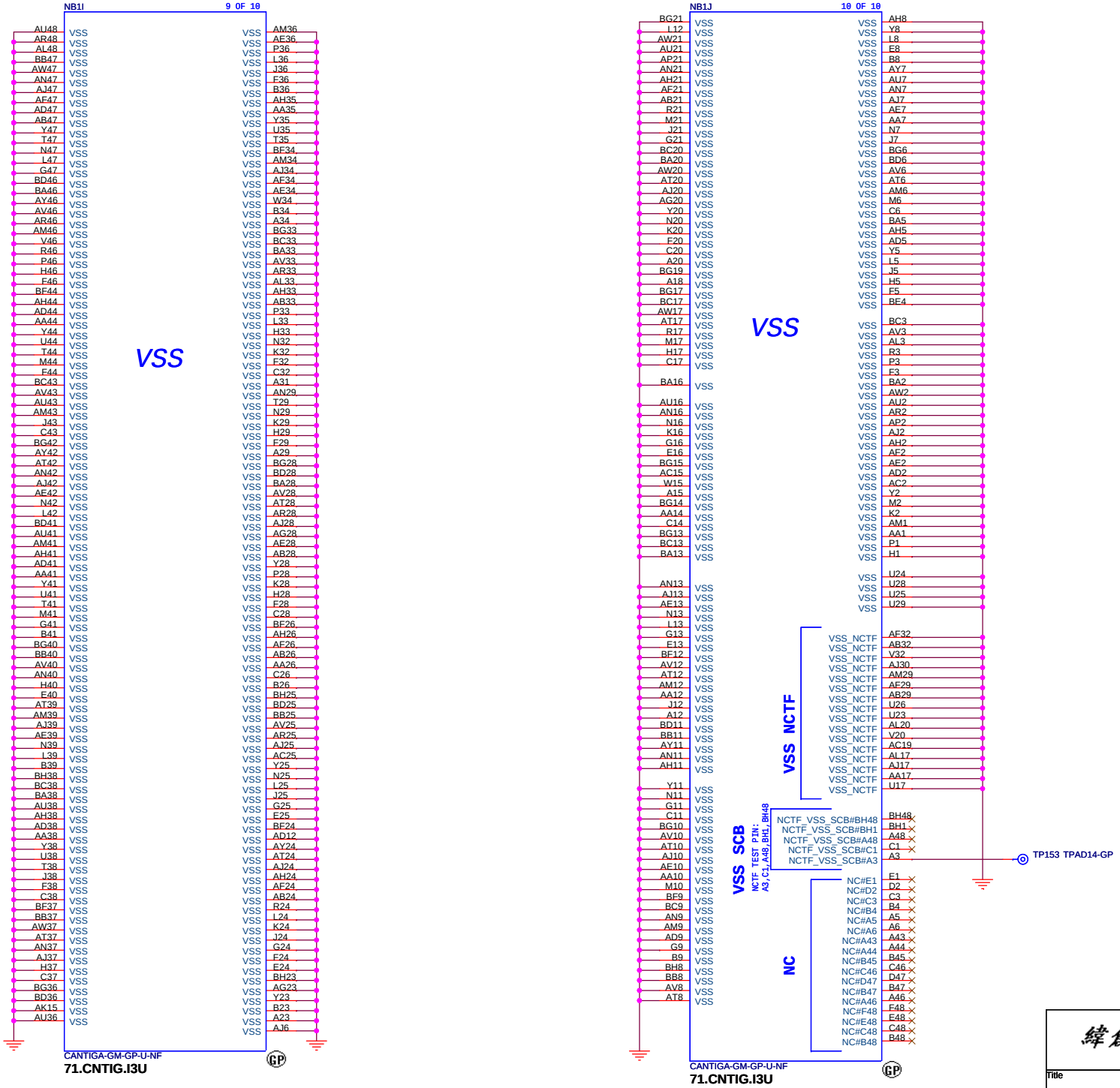

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Title	***Cantiga (6 of 6)***
Size	Document Number: **SM30**
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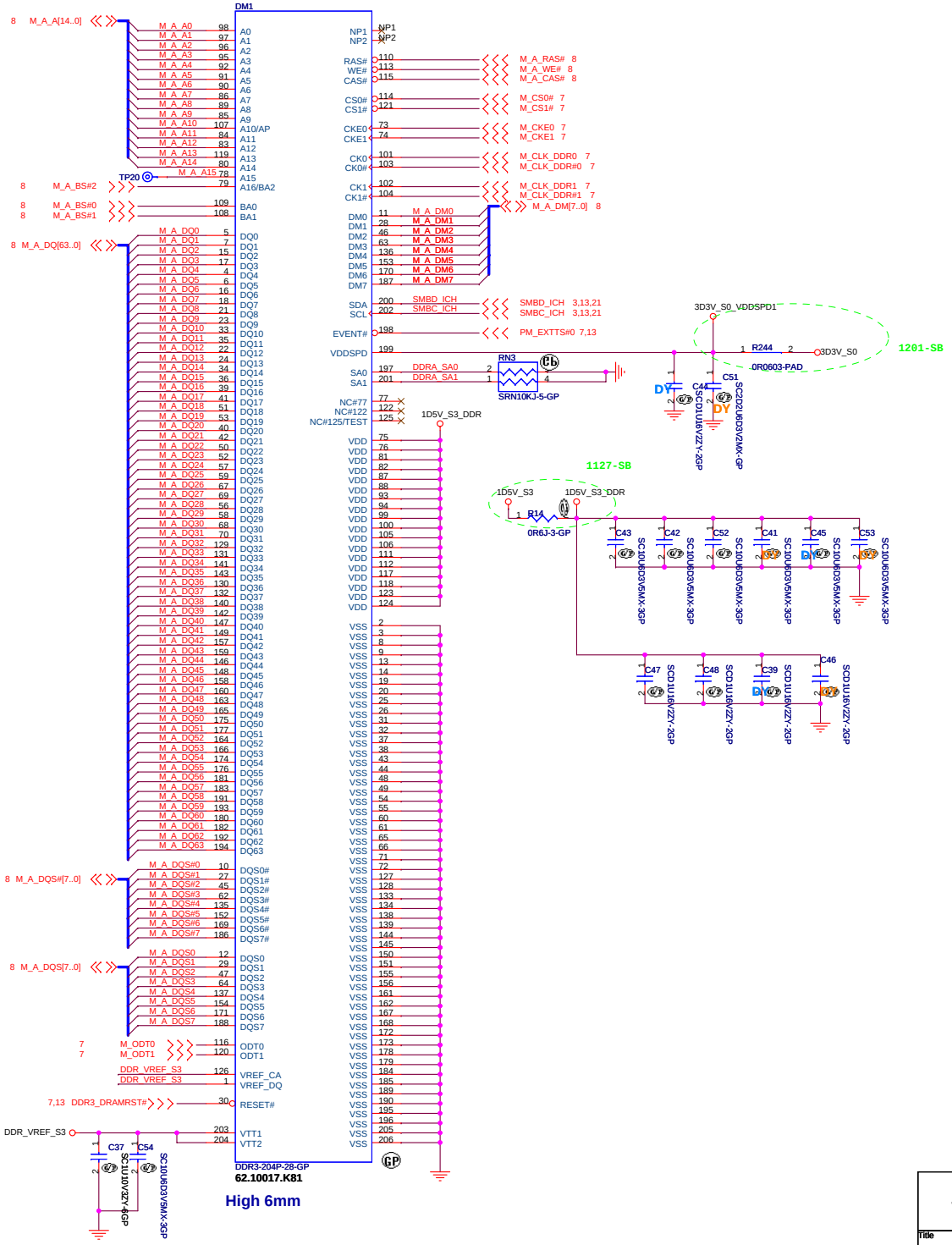
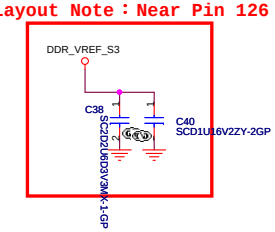
Date: Thursday, December 04, 2008	Sheet 11 of 45

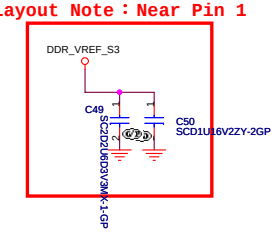
DDR3 SOCKET_1



Layout Note：Near Pin 126



Layout Note：Near Pin 1



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Title	***DDR3 Socket***	
Size	Document Number **SM30**	Rev SB
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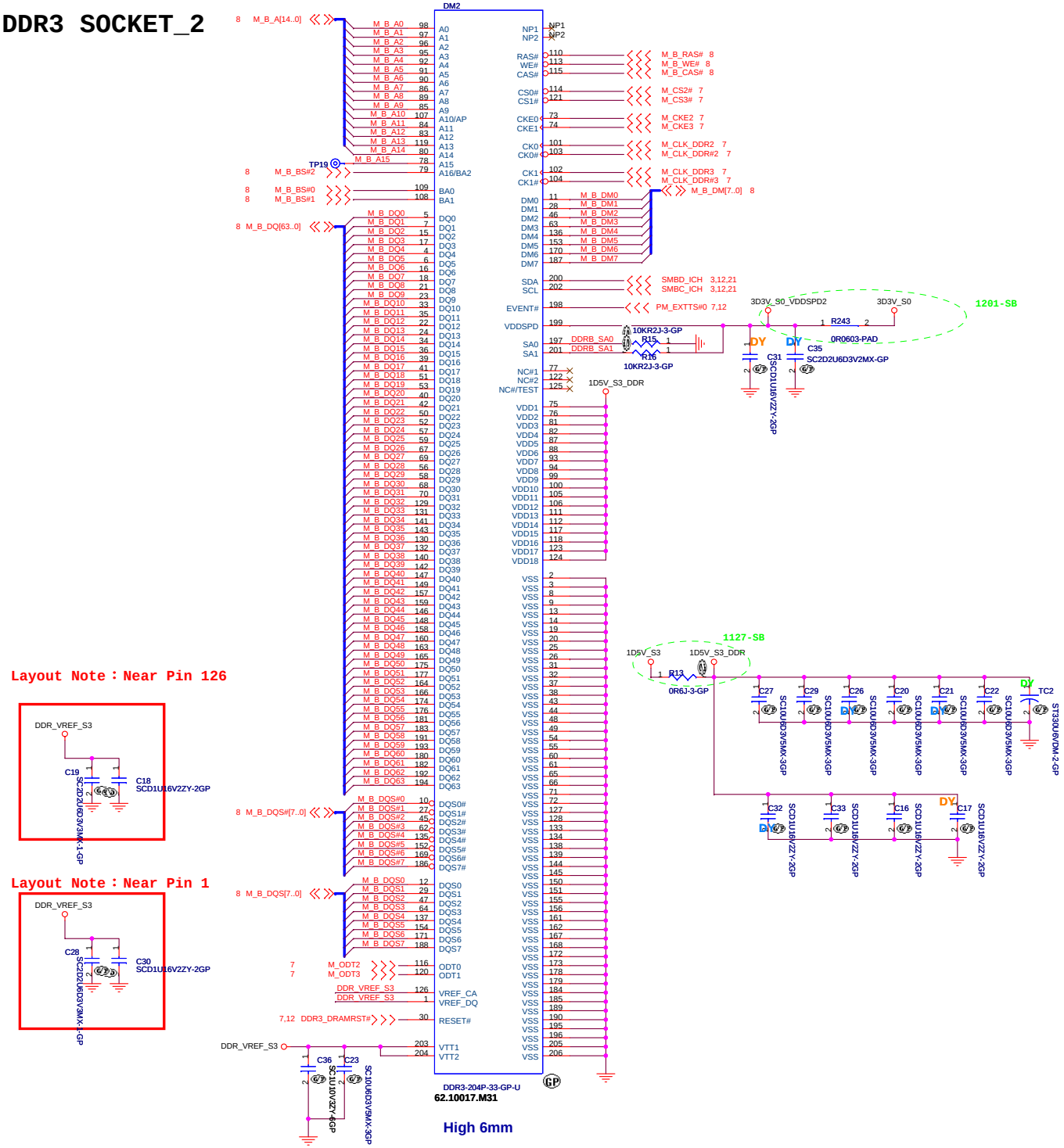
DDR3 SOCKET_2



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Title: ***DDR3 Termination Resistor***

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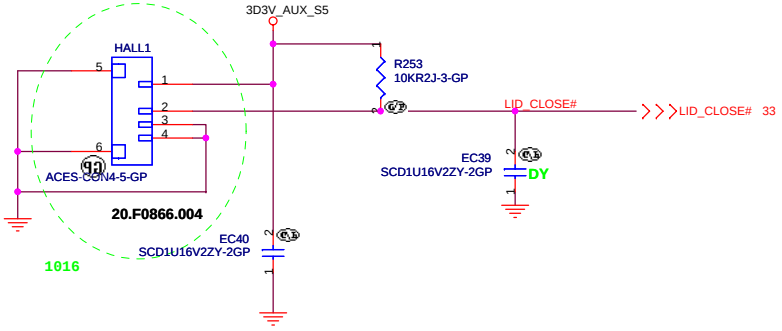
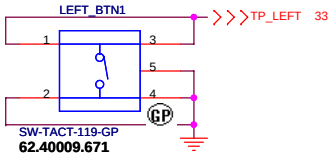
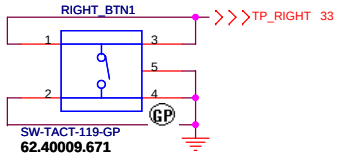
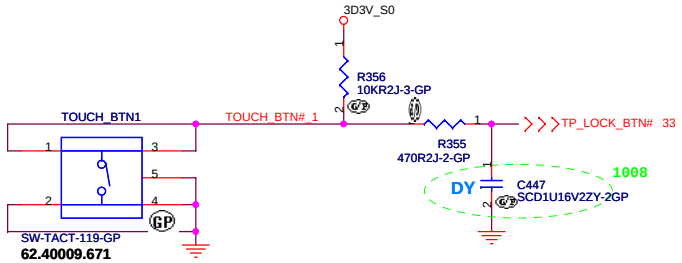
Cover Up Switch

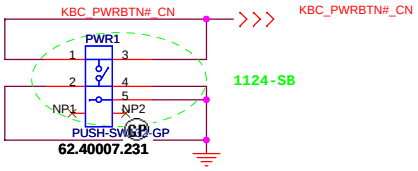


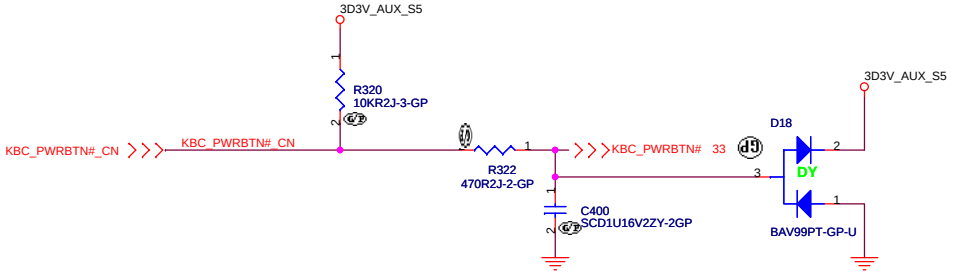
74.00268.A7B
74.00268.C7B











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Title: SWITCH / Button

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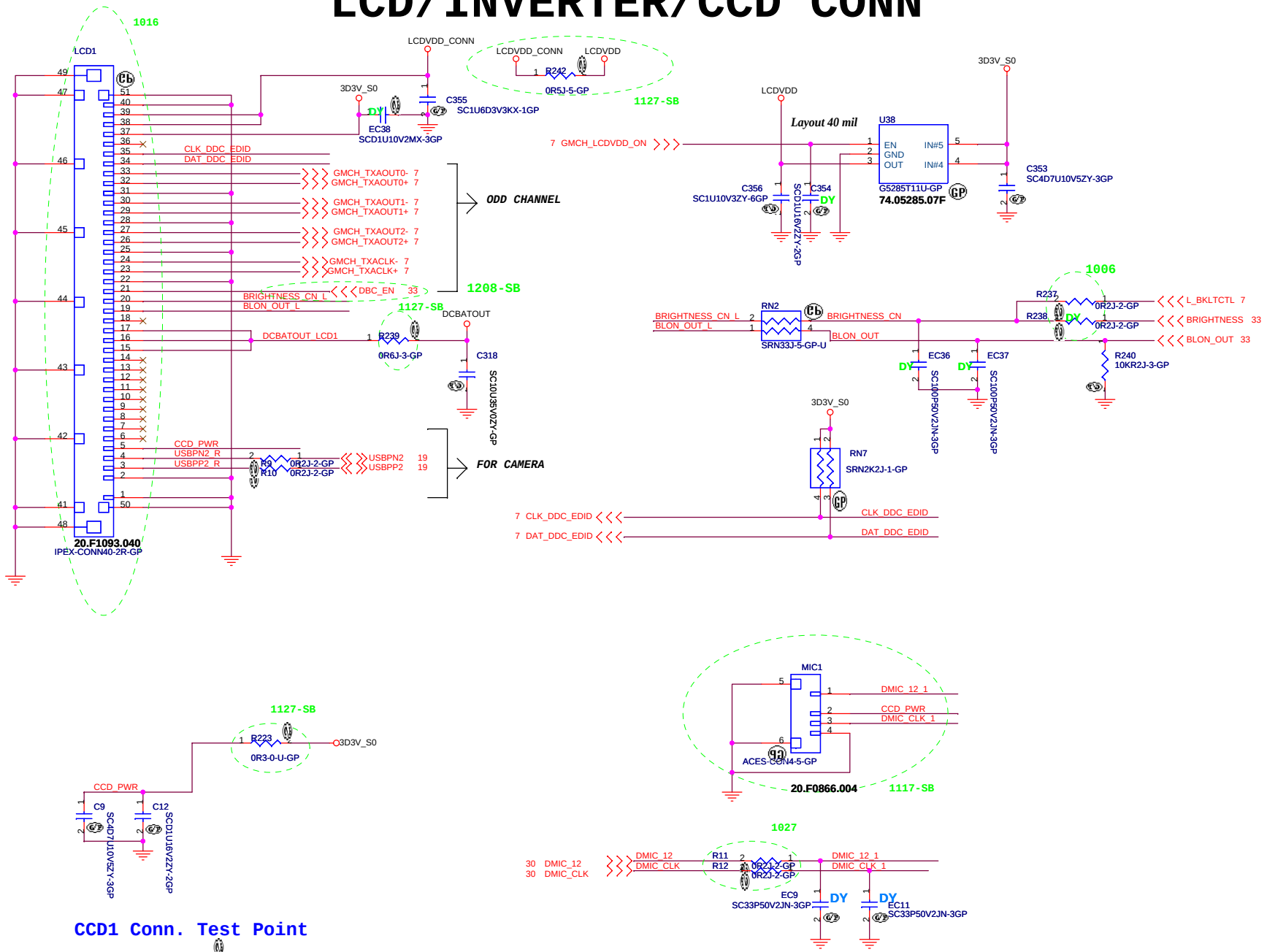
LCD/INVERTER/CCD CONN



SM30

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Title	***LCD CONN***	
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LED

LED 2,3 TOP LIGHTEN
LED 4 SIDE LIGHTEN(OUTSIDE)
LED 5,7 TOP LIGHTEN

Charger LED

1204-SB

RN117 SRN100J-4-GP

DC_BATFULL# Q → Q29 DDTC143ZUA-7-F-GP ← 33 DC_BATFULL

DC_BATFULL# R → CHARGER_LED1 → 3D3V_AUX_S5

CHARGE_LED# R → LED-BO-4-GP

83.00195.G70

CHARGE_LED# Q → Q26 DDTC143ZUA-7-F-GP ← 33 CHARGE_LED

Power LED

FRONT_PWRLED# R → PWR_LED1 → 5V_S0

STDBY_LED# R → LED-BO-4-GP → 3D3V_S5

83.00195.G70

1008

FRONT_PWRLED# Q → Q27 DDTC143ZUA-7-F-GP ← 33 FRONT_PWRLED

STDBY_LED# Q → Q30 DDTC143ZUA-7-F-GP ← 33 STDBY_LED

1204-SB

1106-SB

FRONT_PWRLED# 3R → Q62 DDTC143ZUA-7-F-GP ← 33 AC_LED

1112-SB

RN123 SRN100J-4-GP

FRONT_PWRLED# Q
FRONT_PWRLED# Q

FRONT_PWRLED# 1 → LED2 LED-W-12-GP → 5V_S5

83.00191.D70

FRONT_PWRLED# 2 → LED3 LED-W-12-GP → 5V_S5

83.00191.D70

FRONT_PWRLED# 3 → LED4 LED-Y-74-GP → 5V_S5

83.00110.J70

1204-SB

HDD LED

18 MEDIA_LED# → R201 100R2J-2-GP → MEDIA_LED# 1 → LED6 LED-B-27-U-GP → 5V_S0

83.00190.P70

TP LED

TP_LED# Q → R360 100R2J-2-GP → TP_LED# R → LED9 LED-Y-29-GP → 5V_S0

83.00190.S70

Q23 DDTC143ZUA-7-F-GP ← 33 TP_LOCK_LED

1009

WLAN TEST LED

28 WLAN_LED# → R415 33R2J-2-GP → WLAN_LED# R → R416 75R2J-1-GP → WLAN_LED#_C 35

Q20 2N7002-7F-GP ← 33 WLAN_TEST_LED

84.27002.N31

3G LED

28 3G_LED#_1 → R417 33R2J-2-GP → 3G_LED# R → R418 75R2J-1-GP → 3G_LED#_C 35

Q1 2N7002-7F-GP ← 33 WLAN_TEST_LED

84.27002.N31

1127-SB

POWER CONSUMPTION LED

R260 100R2J-2-GP
NUM_LED# R → NUM_LED# → LED5 LED-B-27-U-GP → 5V_S0

83.00190.P70

Q15 DDTC143ZUA-7-F-GP ← 33 NUM_LED

R225 100R2J-2-GP
CAP_LED# R → CAP_LED# → LED7 LED-B-27-U-GP → 5V_S0

83.00190.P70

Q11 DDTC143ZUA-7-F-GP ← 33 CAP_LED

1113-SB

PWR_CON_LED_C 35

Q12 DDTC143ZUA-7-F-GP ← 33 PWR_CON_LED

<Core Design>

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Title: LED		
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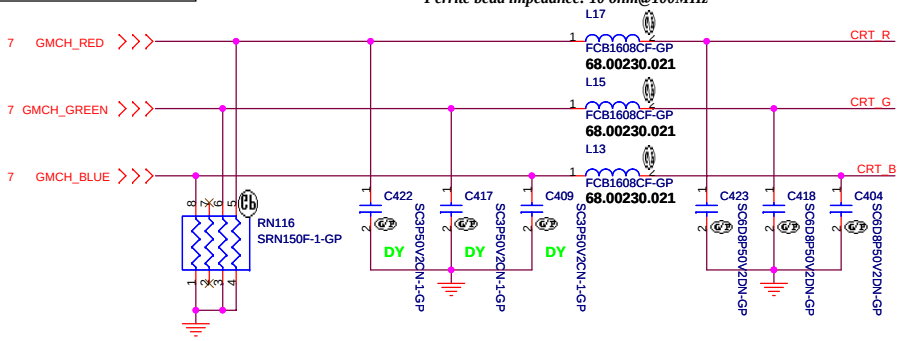
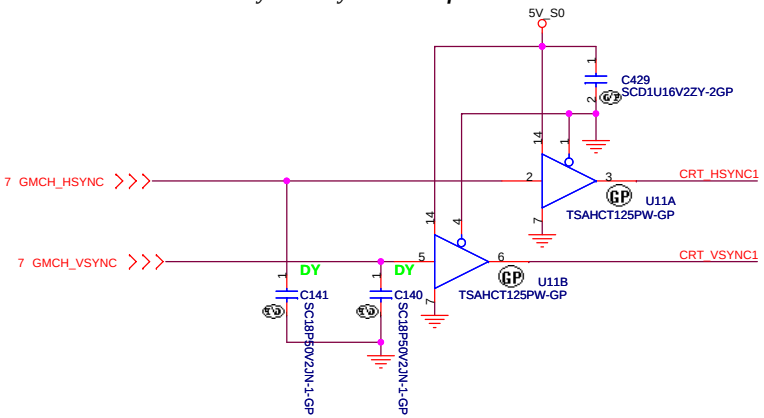
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

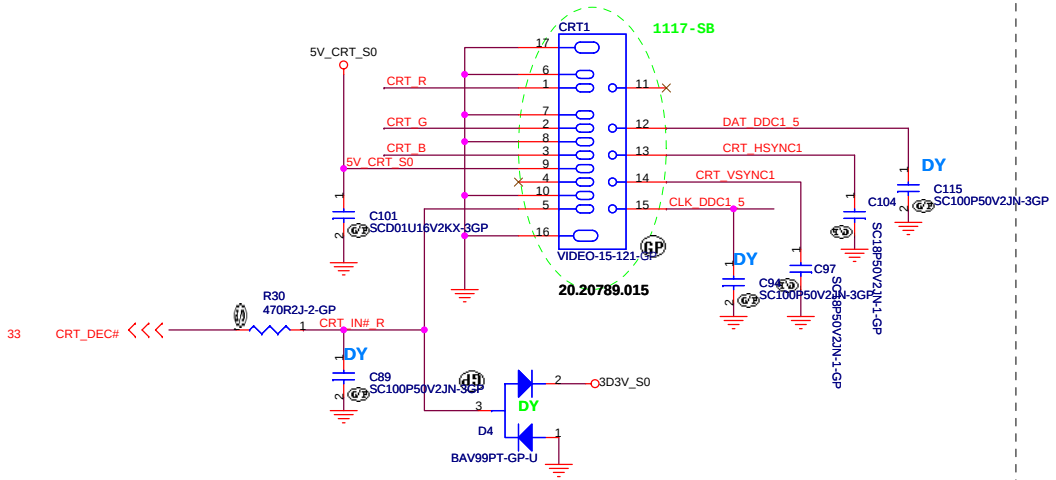


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

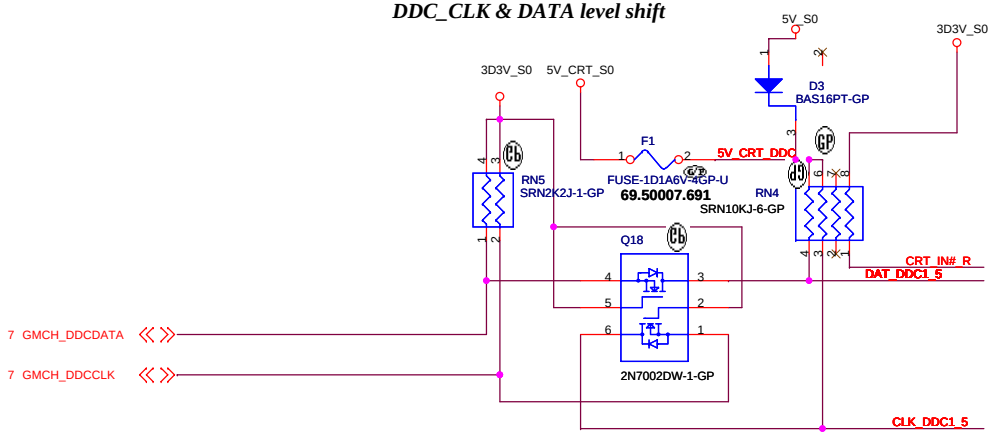
Hsync & Vsync level shift



CRT I/F & CONNECTOR



DDC_CLK & DATA level shift



SM30

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Taipei Hsien 221, Taiwan, R.O.C.

Title	***CRT CONN***	
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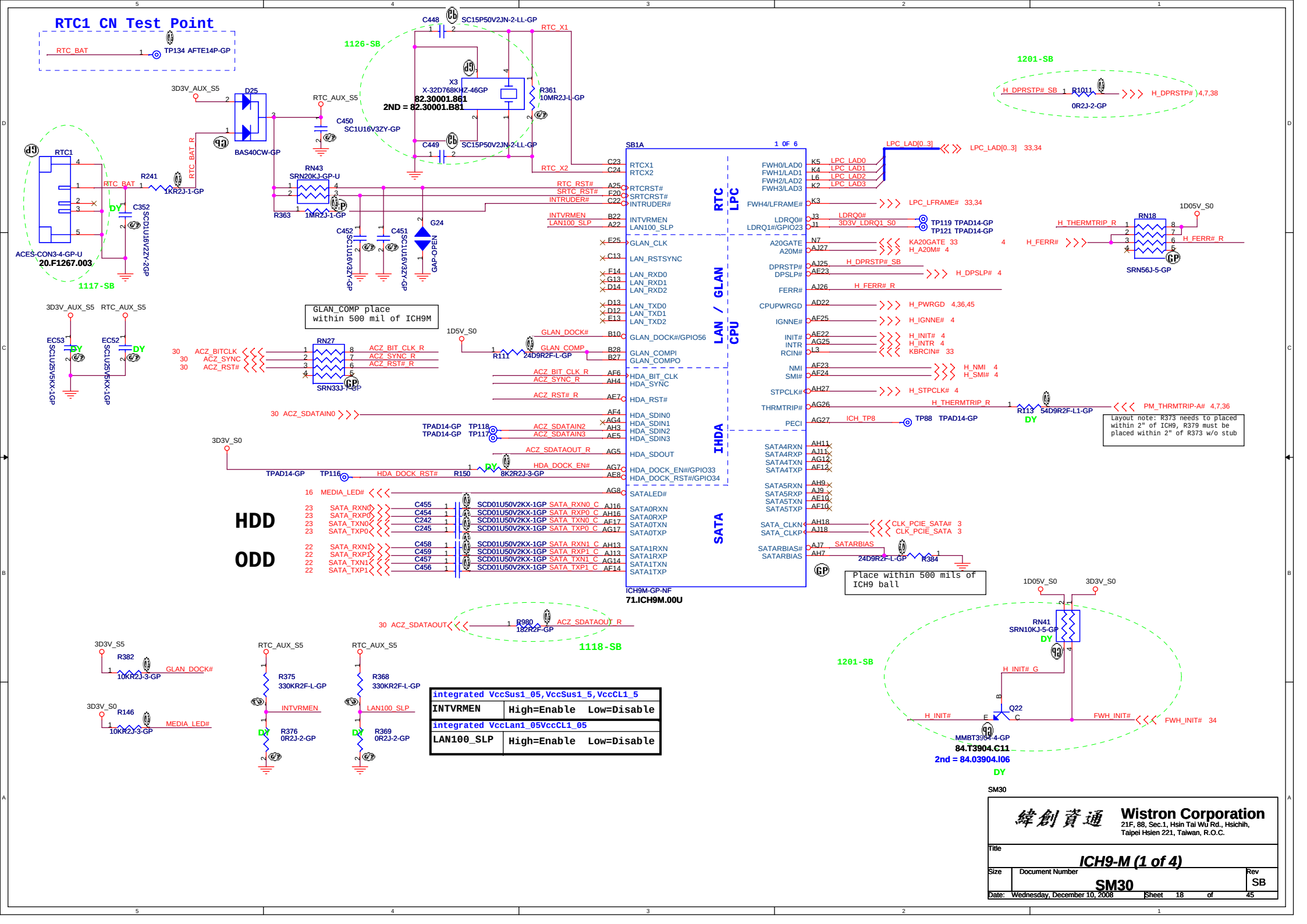
RTC1 CN Test Point
RTC_BAT
TP134 AFTE14P-GP
1126-SB
C448 SC15P50V2JN-2-LL-GP
RTC_X1
X3
X-32D768KHZ-46GP
82.30001.861
2ND = 82.30001.B81
R361 10MR2J-L-GP
C449 SC15P50V2JN-2-LL-GP
RTC_X2
3D3V_AUX_S5
D25
BAS40CW-GP
RTC_AUX_S5
C450 SC1U16V3ZY-GP
RTC_BAT_R
RTC1
ACES-CON3-4-GP-U
20.F1267.003
1117-SB
R241 1KR2J-1-GP
C352 SC1U16V2ZY-2GP
RN43 SRN20KJ-GP-U
R363 1MR2J-1-GP
C452 SC1U16V3ZY-GP
C451 SC1U16V3ZY-GP
G24 GAP-OPEN
SB1A
1 OF 6
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
RTC
LPC
GLAN
LAN / CPU
IHDA
SATA
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
ICH9M-GP-NF
71.ICH9M.00U
LPC_LAD[0..3]
LPC_LAD[0..3] 33,34
LPC_LFRAME# 33,34
TP119 TPAD14-GP
TP121 TPAD14-GP
KA20GATE 33
H_A20M# 4
H_DPRSTP# SB
H_DPSLP# 4
H_FERR# R
H_PWRGD 4,36,45
H_IGNNE# 4
H_INIT# 4
H_INTR 4
KBRCIN# 33
H_NMI 4
H_SMI# 4
H_STPCLK# 4
H_THERMTRIP_R
PM_THRMTRIP-A# 4,7,36
ICH_TP8
TP88 TPAD14-GP
CLK_PCIE_SATA# 3
CLK_PCIE_SATA 3
SATARBIAS
1201-SB
H_DPRSTP# SB
R1011 0R2J-2-GP
H_DPRSTP# 4,7,38
RN18 SRN56J-5-GP
1D05V_S0
H_FERR#
H_THERMTRIP_R
R113 54D9R2F-L1-GP
DY
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
GLAN_COMP place within 500 mil of ICH9M
3D3V_AUX_S5
RTC_AUX_S5
EC53 SC1U25V5KX-1GP
EC52 SC1U25V5KX-1GP
RN27 SRN33J-7-GP
ACZ_BITCLK
ACZ_SYNC
ACZ_RST#
ACZ_BIT_CLK_R
ACZ_SYNC_R
ACZ_RST#_R
1D5V_S0
R111 24D9R2F-L-GP
GLAN_DOCK#
GLAN_COMP
ACZ_SDATAIN0
TPAD14-GP TP118
TPAD14-GP TP117
ACZ_SDATAIN2
ACZ_SDATAIN3
3D3V_S0
ACZ_SDATAOUT_R
TPAD14-GP TP116
HDA_DOCK_RST#
R150 8K2R2J-3-GP
HDA_DOCK_EN#
MEDIA_LED#
HDD
ODD
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
C455 SCD01U50V2KX-1GP SATA_RXN0_C
C454 SCD01U50V2KX-1GP SATA_RXP0_C
C242 SCD01U50V2KX-1GP SATA_TXN0_C
C245 SCD01U50V2KX-1GP SATA_TXP0_C
C458 SCD01U50V2KX-1GP SATA_RXN1_C
C459 SCD01U50V2KX-1GP SATA_RXP1_C
C457 SCD01U50V2KX-1GP SATA_TXN1_C
C456 SCD01U50V2KX-1GP SATA_TXP1_C
ACZ_SDATAOUT
R980 182R2F-GP
1118-SB
Place within 500 mils of ICH9 ball
3D3V_S5
R382 10KR2J-3-GP
GLAN_DOCK#
3D3V_S0
R146 10KR2J-3-GP
MEDIA_LED#
RTC_AUX_S5
R375 330KR2F-L-GP
INTVRMEN
R376 0R2J-2-GP
R368 330KR2F-L-GP
LAN100_SLP
R369 0R2J-2-GP
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
1201-SB
RN41 SRN10KJ-5-GP
H_INIT# G
Q22 MMBT3904-4-GP
H_INIT#
FWH_INIT#
FWH_INIT# 34
84.T3904.C11
2nd = 84.03904.I06
DY
SM30
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)
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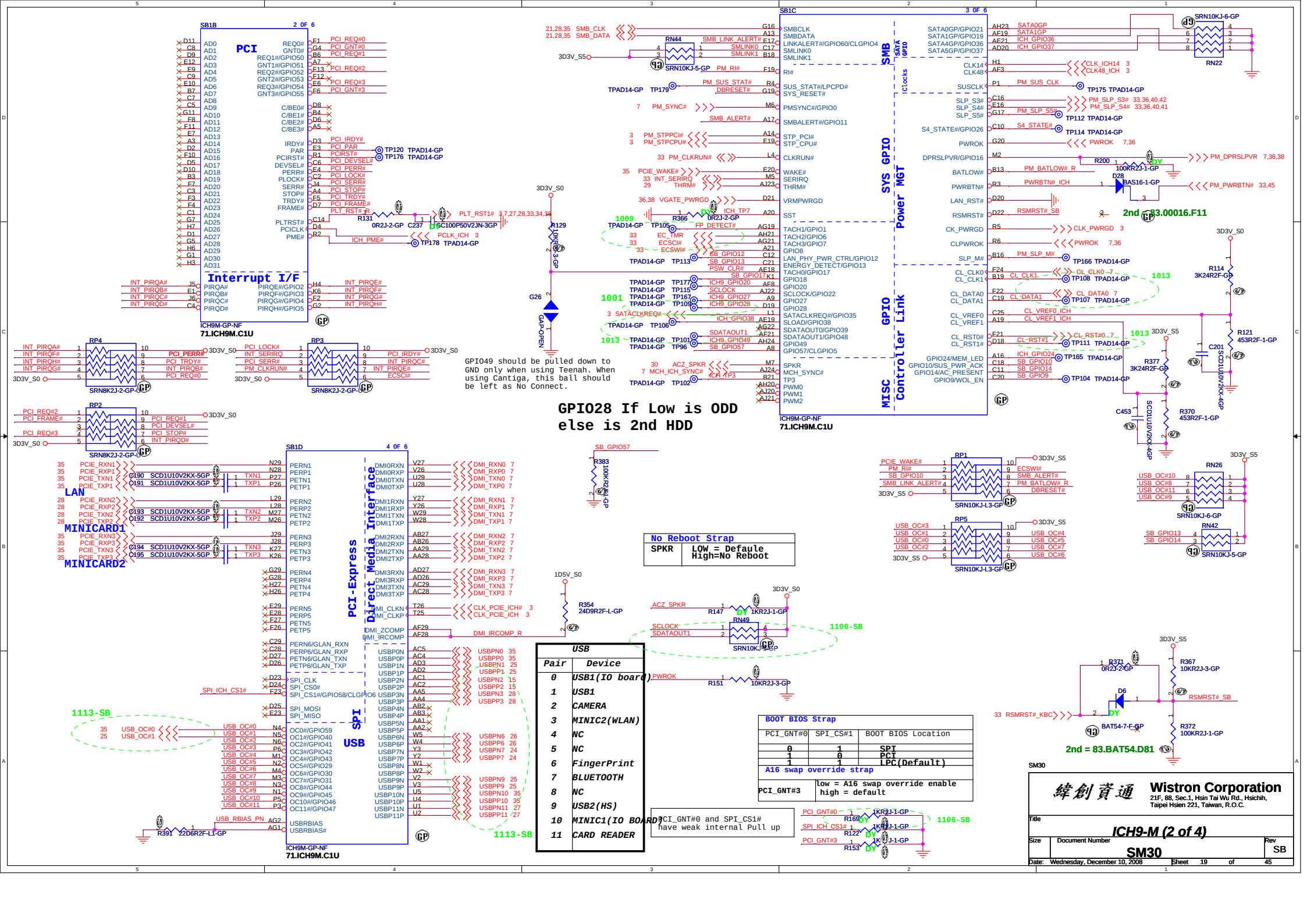
SB1B 2 OF 6
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.C1U
SB1C 3 OF 6
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-GP-NF
71.ICH9M.C1U
SB1D 4 OF 6
PCI-Express
Direct Media Interface
SPI
USB
ICH9M-GP-NF
71.ICH9M.C1U
GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
GPIO28 If Low is ODD else is 2nd HDD
No Reboot Strap
SPKR LOW = Defaule High=No Reboot
USB
Pair Device
0 USB1(IO board)
1 USB1
2 CAMERA
3 MINIC2(WLAN)
4 NC
5 NC
6 FingerPrint
7 BLUETOOTH
8 NC
9 USB2(HS)
10 MINIC1(IO BOARD)
11 CARD READER
BOOT BIOS Strap
PCI_GNT#0 SPI_CS#1 BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3 low = A16 swap override enable high = default
PCI_GNT#0 and SPI_CS1# have weak internal Pull up
2nd = 83.00016.F11
2nd = 83.BAT54.D81
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Title
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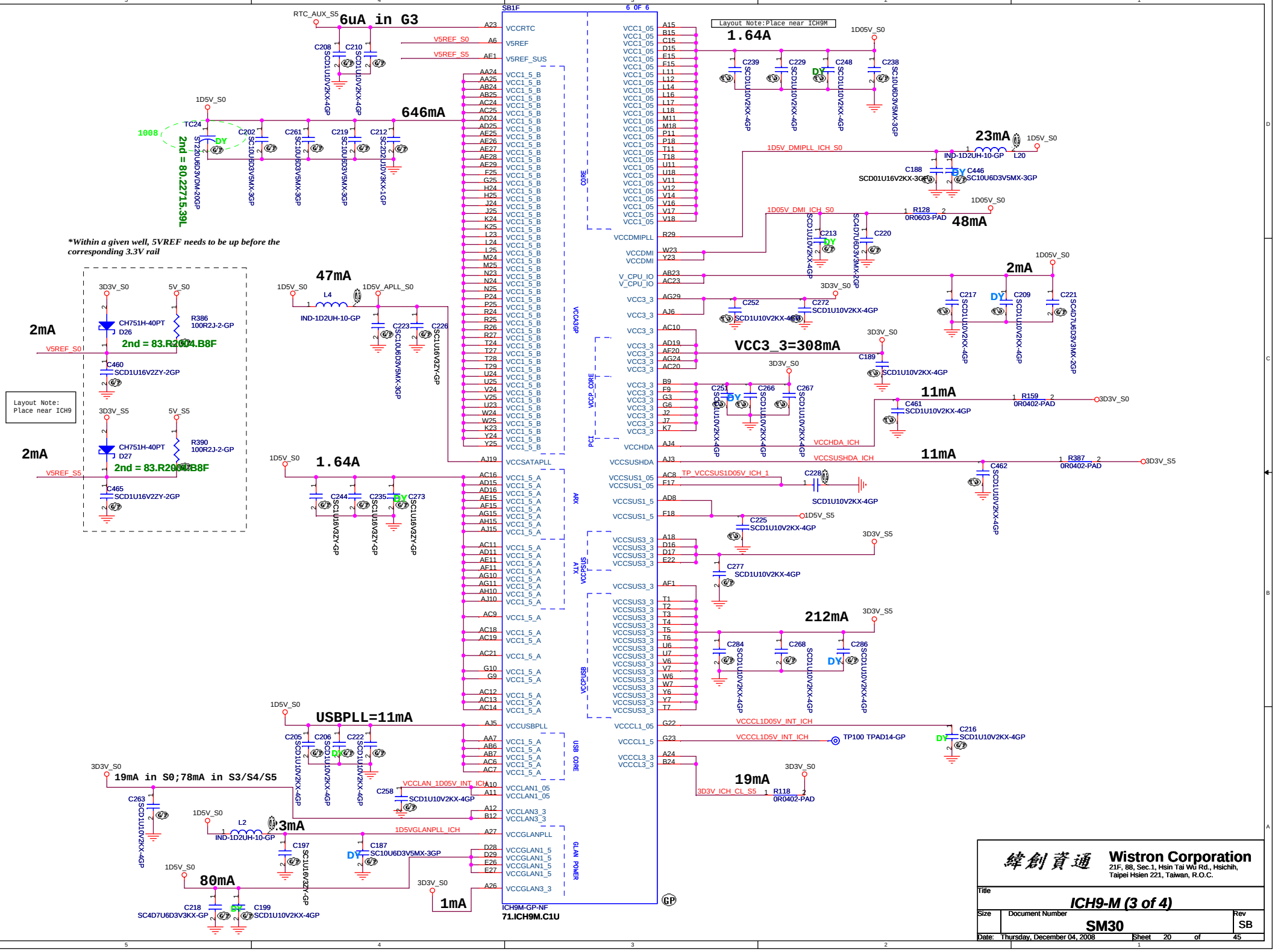
SB1F
6 OF 6
ICH9M-GP-NF
71.ICH9M.C1U
6uA in G3
RTC_AUX_S5
V5REF_S0
V5REF_S5
646mA
1D5V_S0
1008
2nd = 80.22715.39L
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
2mA
3D3V_S0
5V_S0
CH751H-40PT
D26
R386
100R2J-2-GP
2nd = 83.R2004.B8F
C460
SCD1U16V2ZY-2GP
Layout Note:
Place near ICH9
3D3V_S5
5V_S5
D27
R390
2nd = 83.R2004.B8F
C465
47mA
L4
IND-1D2UH-10-GP
1.64A
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
3mA
80mA
1mA
SC4D7U6D3V3KX-GP
SCD1U10V2KK-4GP
SC10U6D3V5MX-3GP
SC1U16V2ZY-GP
SC2D2U10V3KX-1GP
SC220U6D3V5M-20GP
Layout Note:Place near ICH9M
1.64A
23mA
IND-1D2UH-10-GP
SCD01U16V2KX-3GP
SC10U6D3V5MX-3GP
48mA
0R0603-PAD
2mA
VCC3_3=308mA
11mA
0R0402-PAD
212mA
19mA
3D3V_ICH_CL_S5
TP100 TPAD14-GP
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
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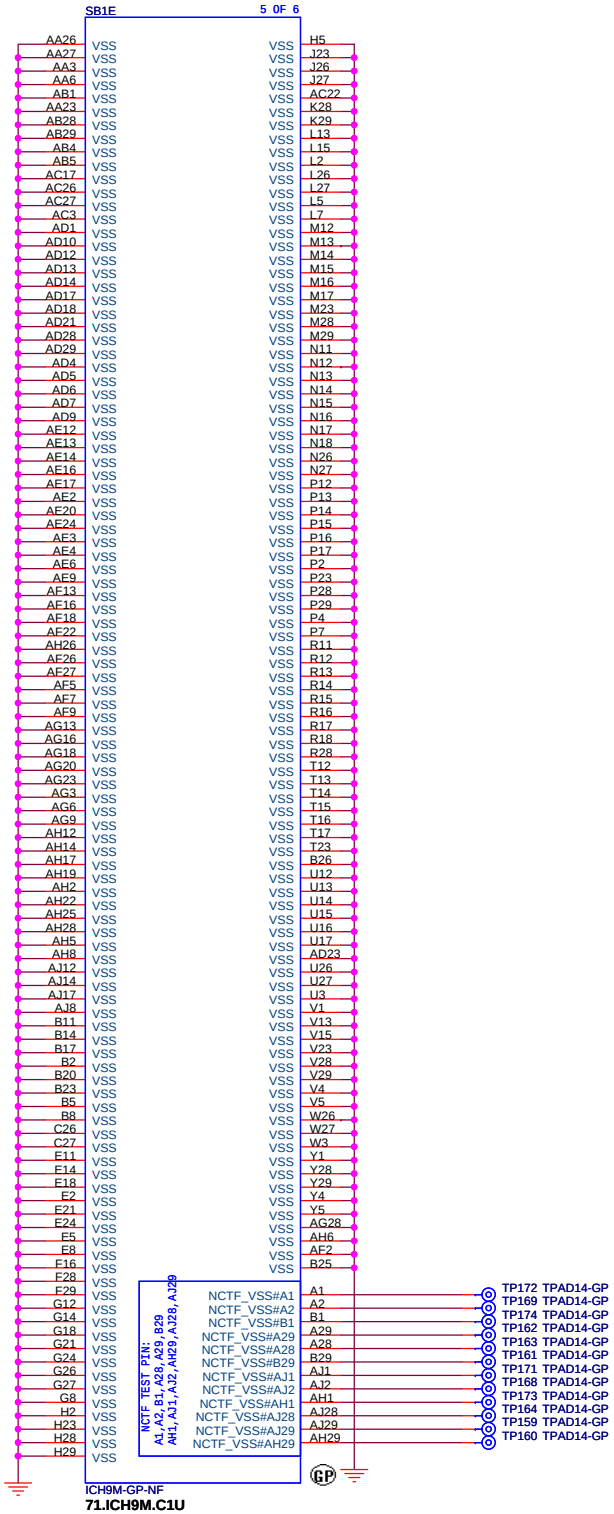

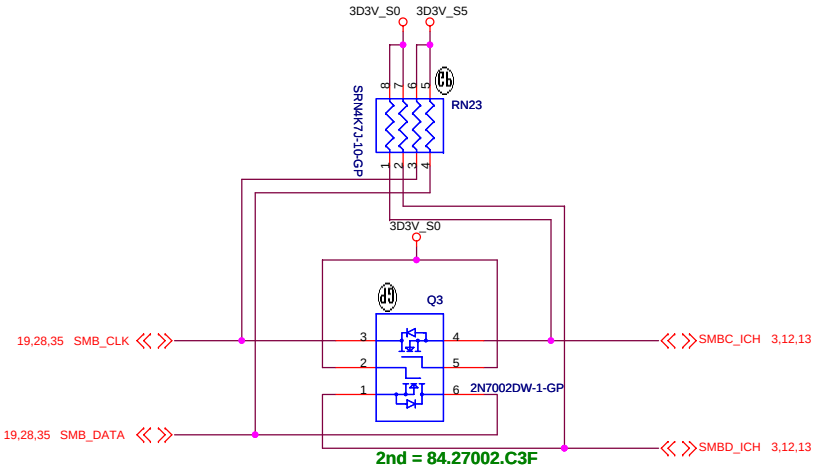

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*ICH9-M (4 of 4)*	
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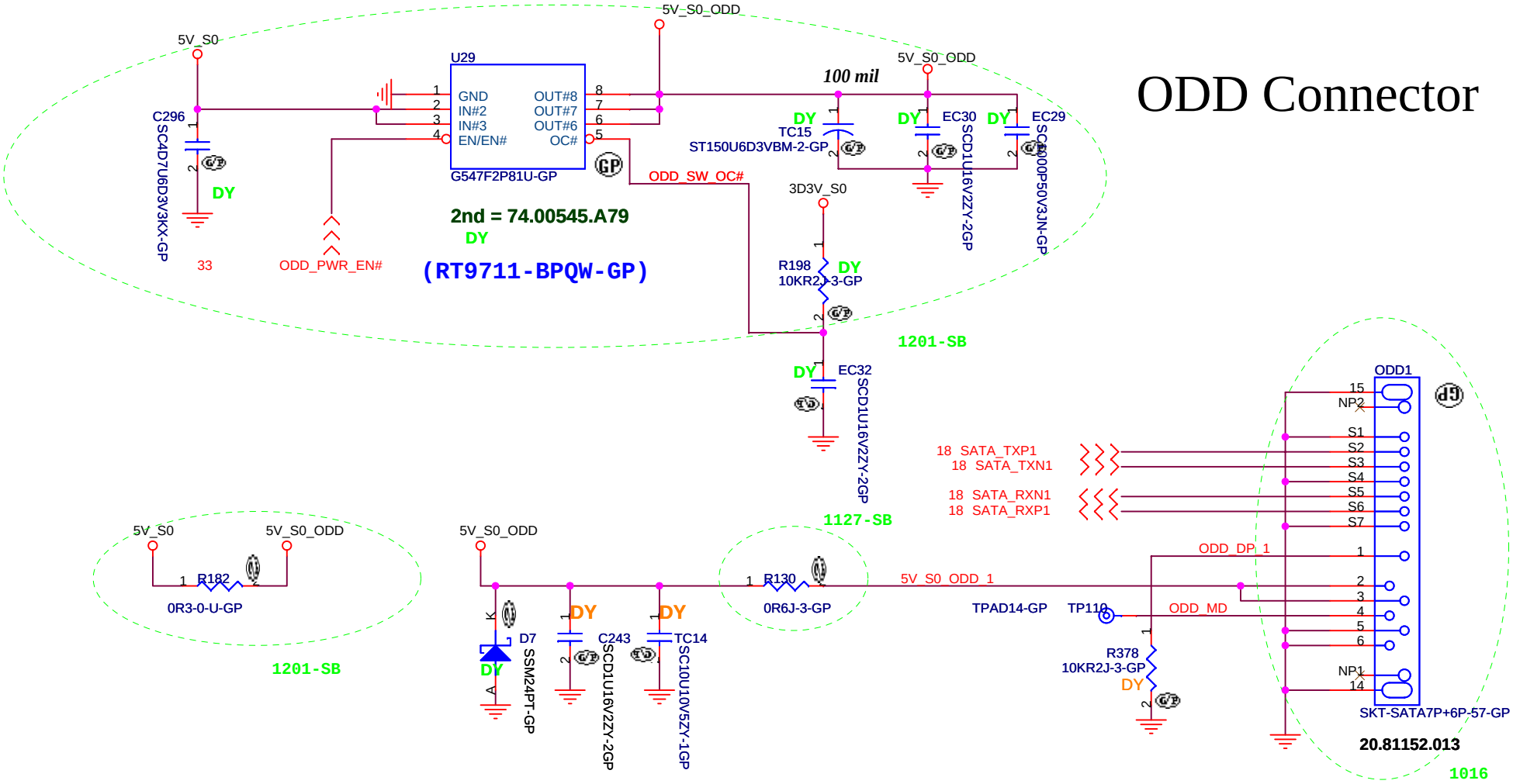
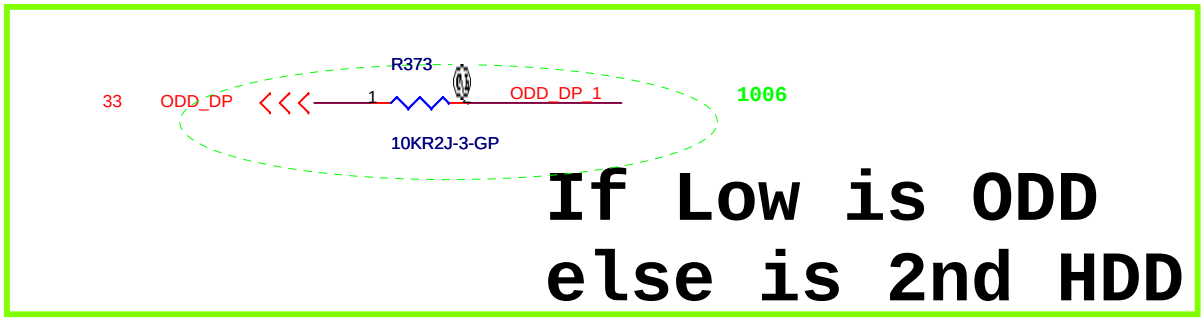
ODD Connector





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Title: ODD		
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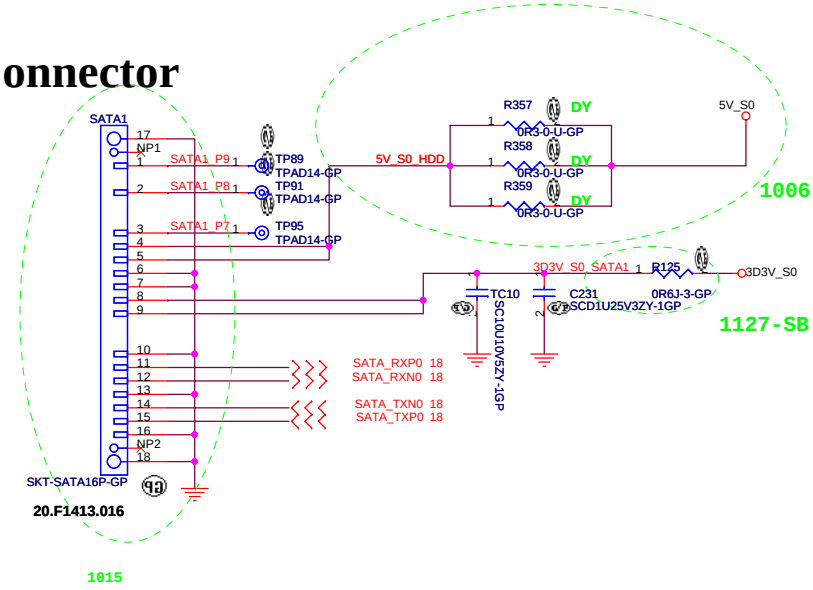
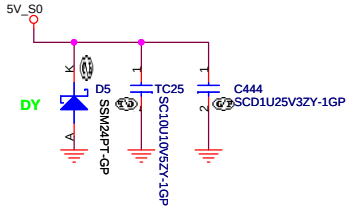
SATA Connector





SM30

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *HDD CONN*		
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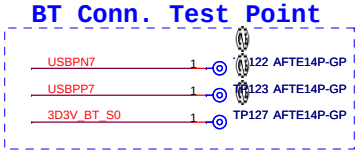
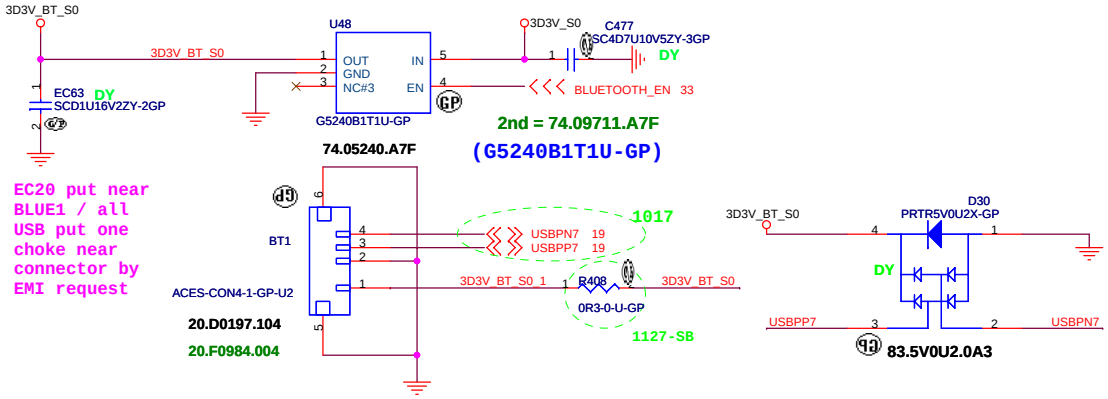
BLUETOOTH MODULE





Need check conn.

SM30

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BLUETOOTH		
Size	Document Number: SM30	Rev: SB
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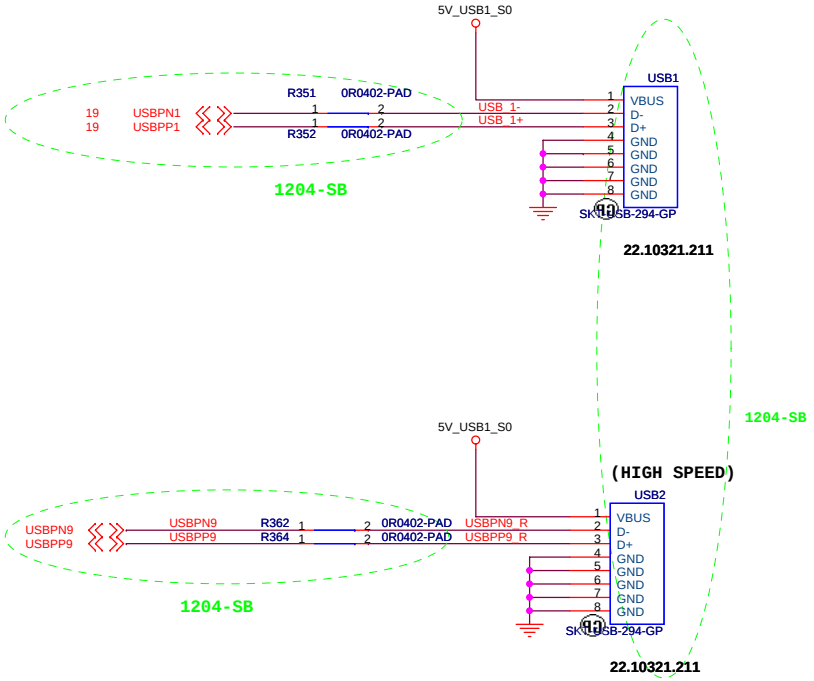

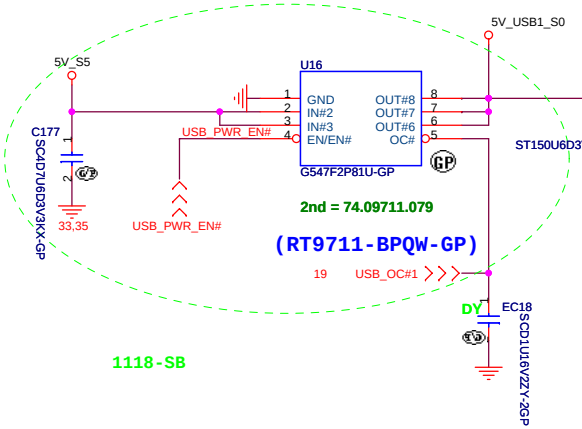

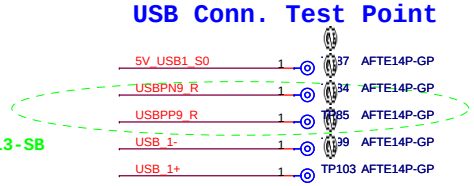

SM30

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Title: USB

Size	Document Number	Rev
	SM30	SB

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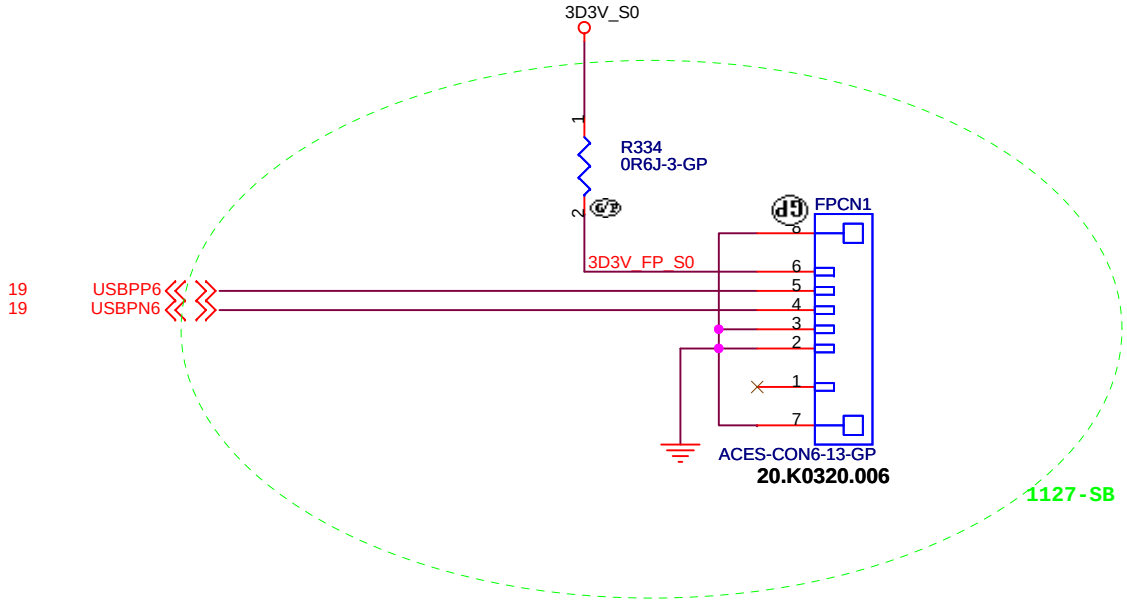
Finger printer

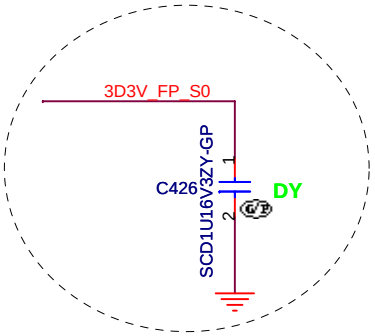
FP Conn. Test Point

3D3V_FP_S0 — 1 — TP148 AFTE14P-GP

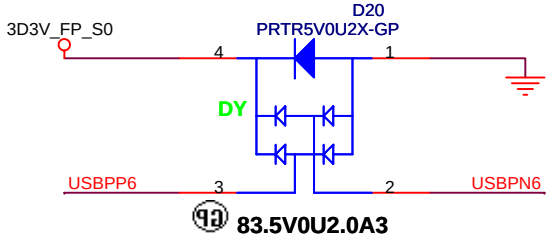
USBPP6 — 1 — TP146 AFTE14P-GP

USBPN6 — 1 — TP145 AFTE14P-GP





For EMI



SM30

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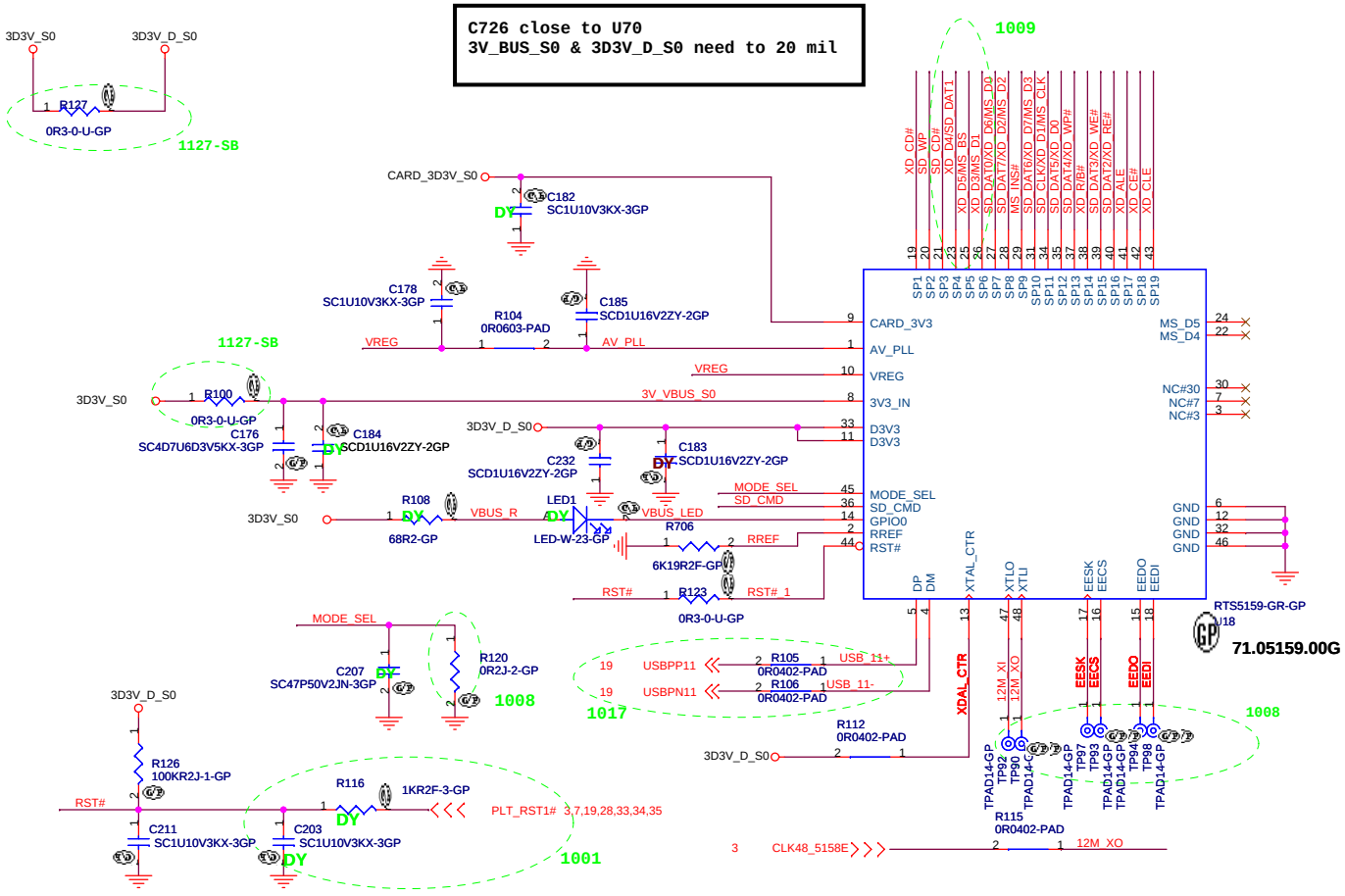
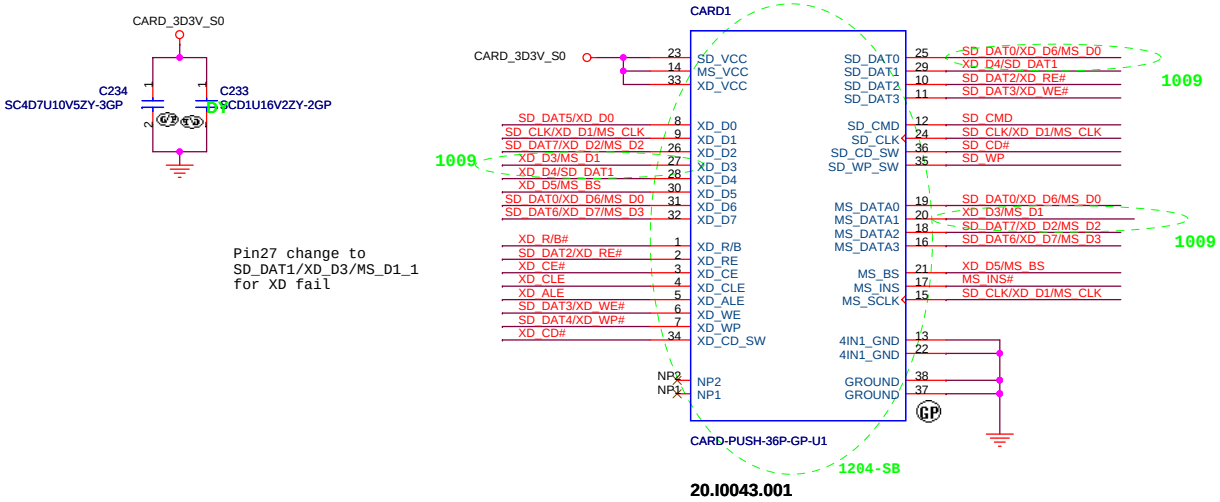
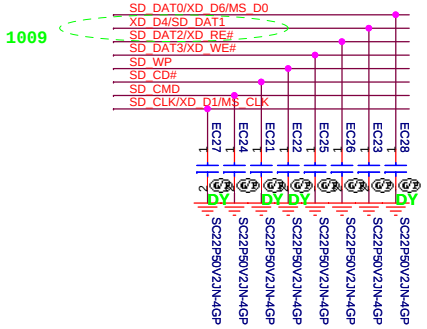
Title: *Finger Printer*		
Size	Document Number: SM30	Rev: SB
Date: Wednesday, December 10, 2008	Sheet 26 of 45	

C726 close to U70
3V_BUS_S0 & 3D3V_D_S0 need to 20 mil



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)





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Title: CARDREADER- RTS5158E

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	SM30	SB

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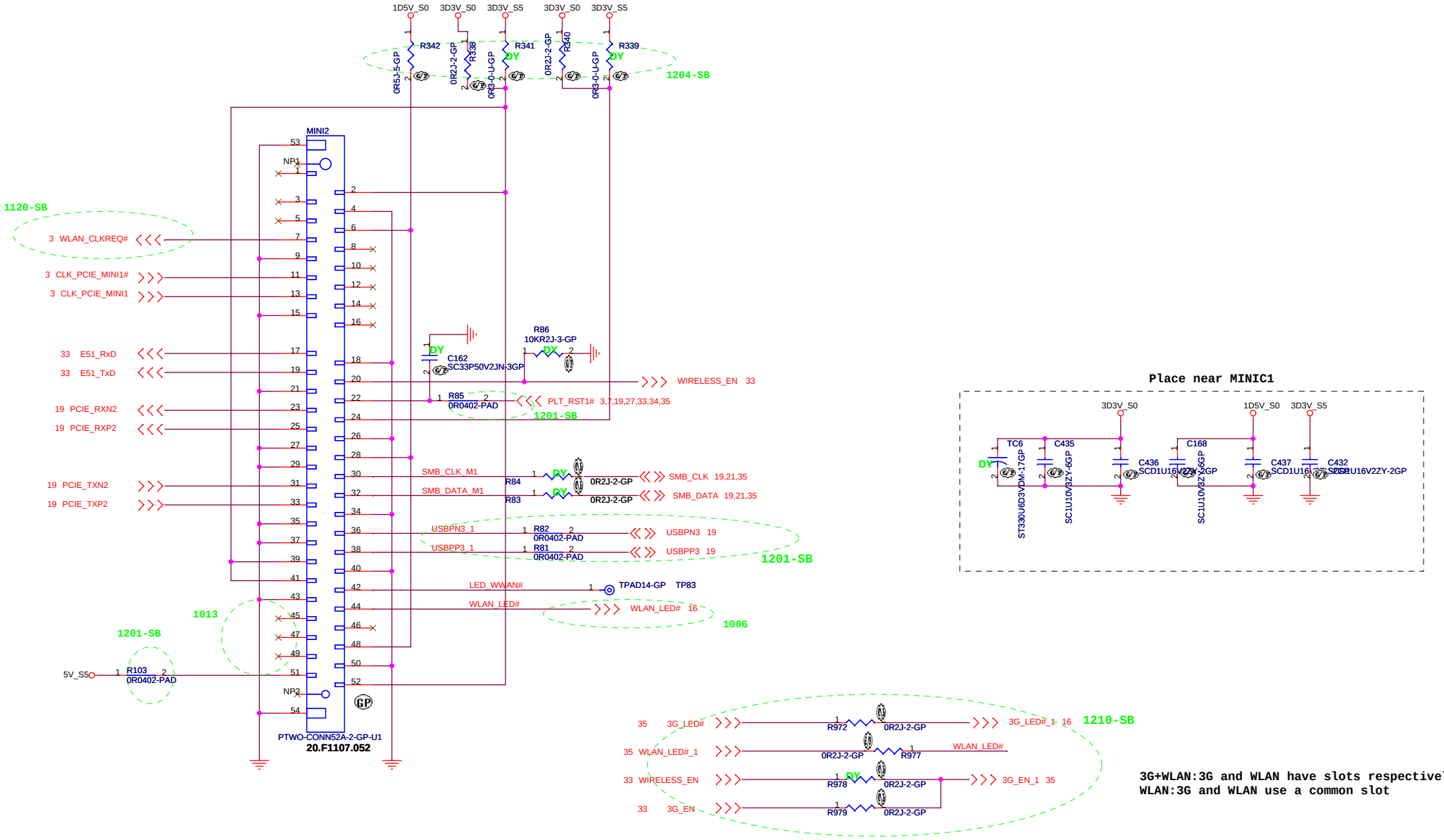
Mini Card Connector(WLAN)



SM30

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD**

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A3	SM30	SB

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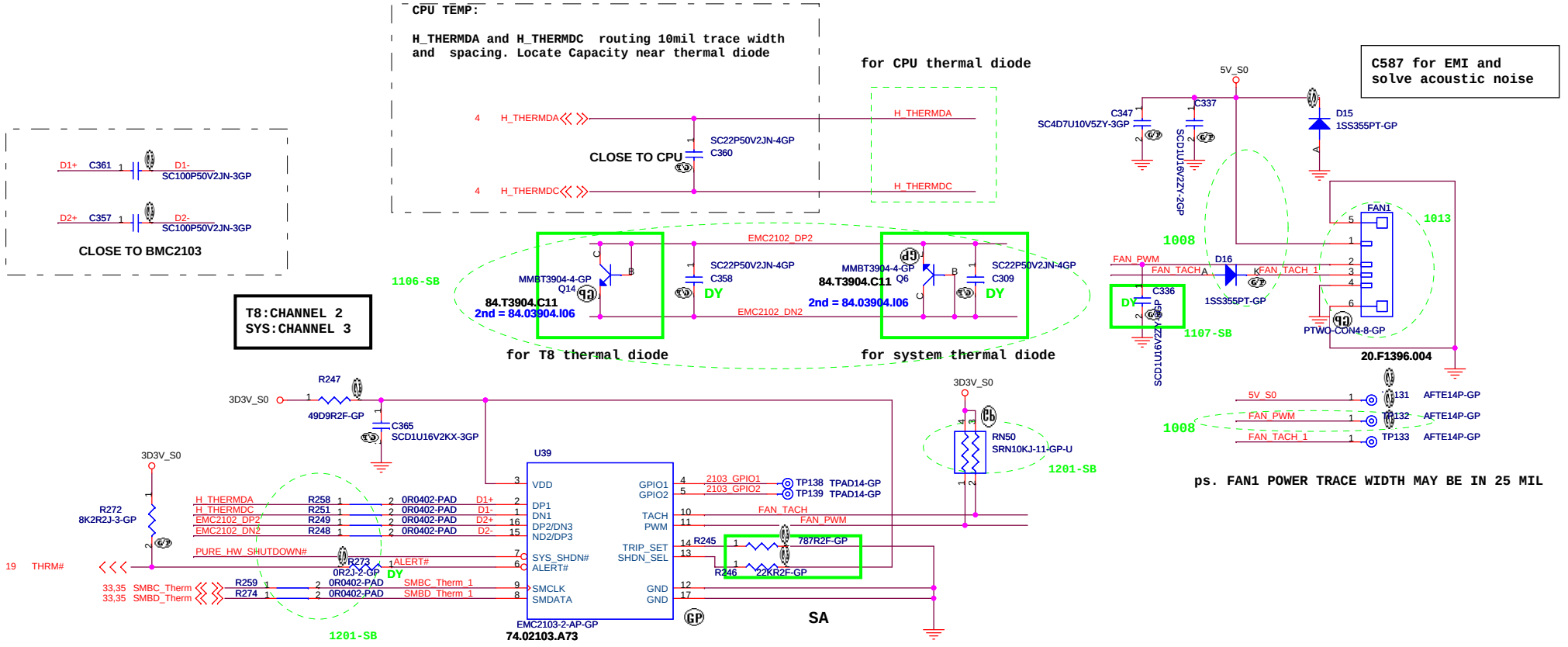

SM30

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

Size	Document Number	Rev
	SM30	SB

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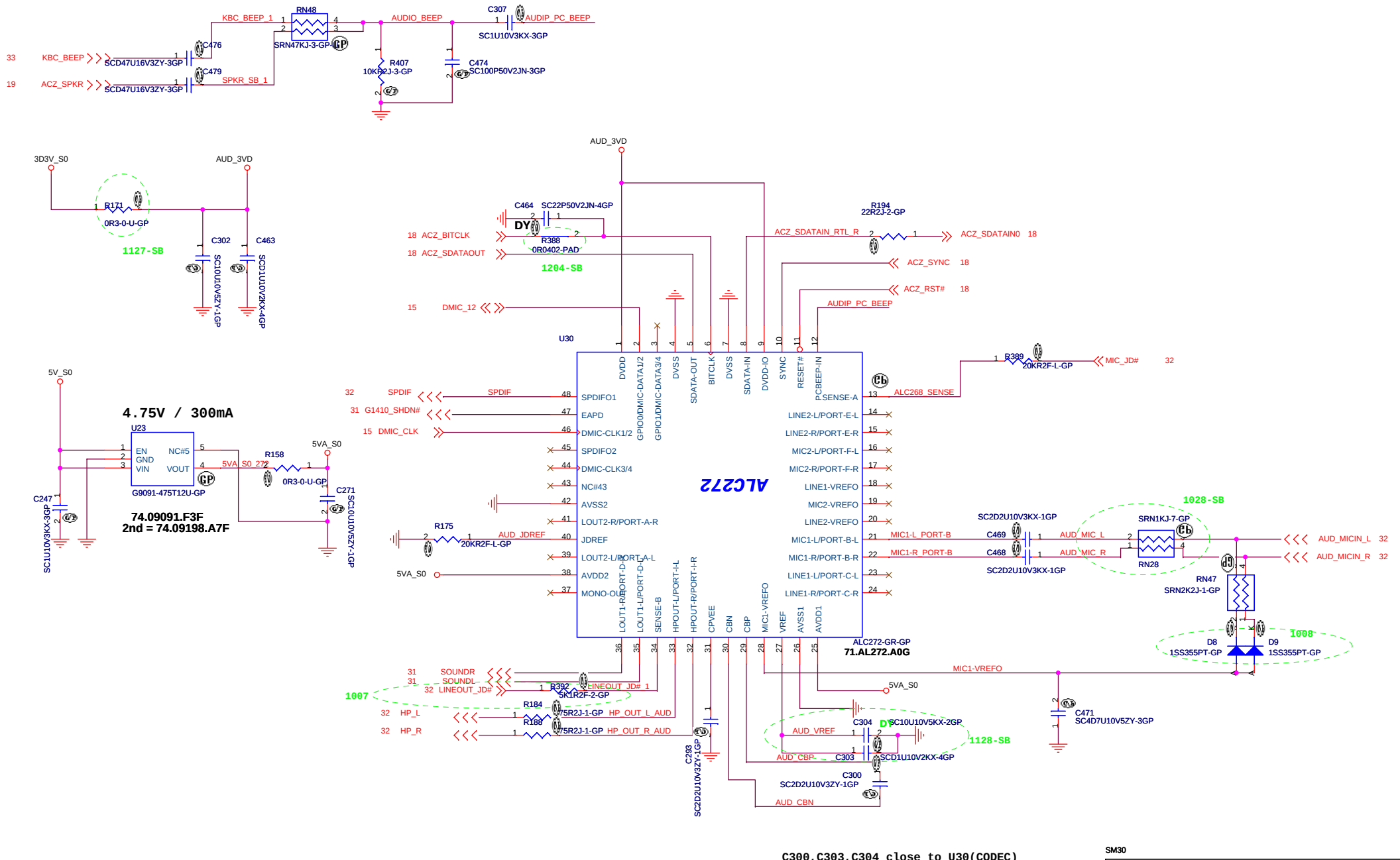

C300,C303,C304 close to U30(CODEC)

SM30

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Azalia codec ALC268***

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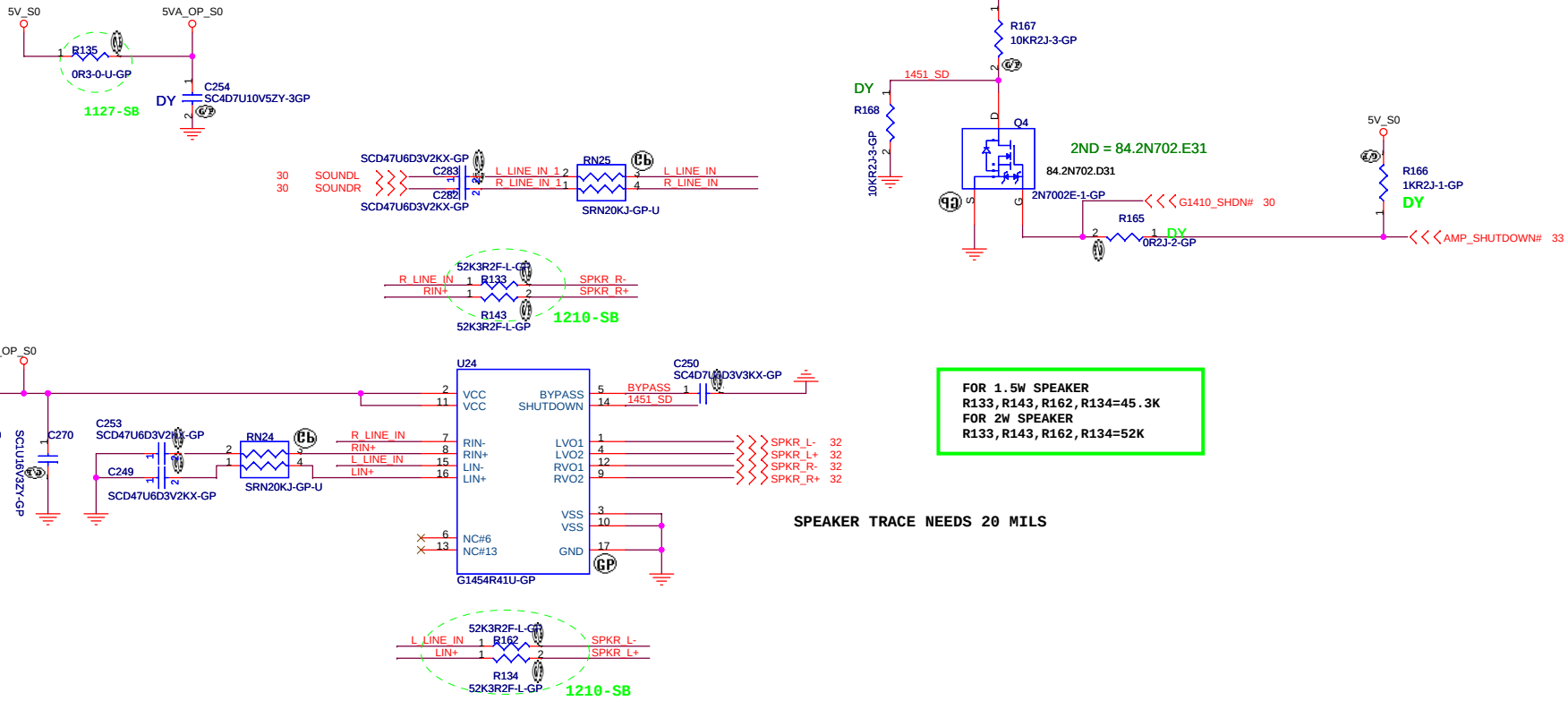
AUDIO OP AMPLIFIER



FOR 1.5W SPEAKER
R133,R143,R162,R134=45.3K
FOR 2W SPEAKER
R133,R143,R162,R134=52K

SPEAKER TRACE NEEDS 20 MILS

SM30

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Title	*AUDIO AMP*	
Size	Document Number: SM30	Rev: SB
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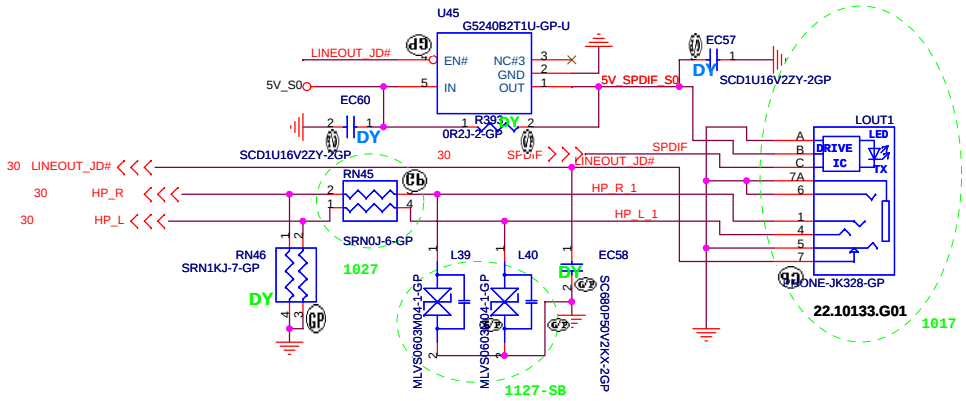
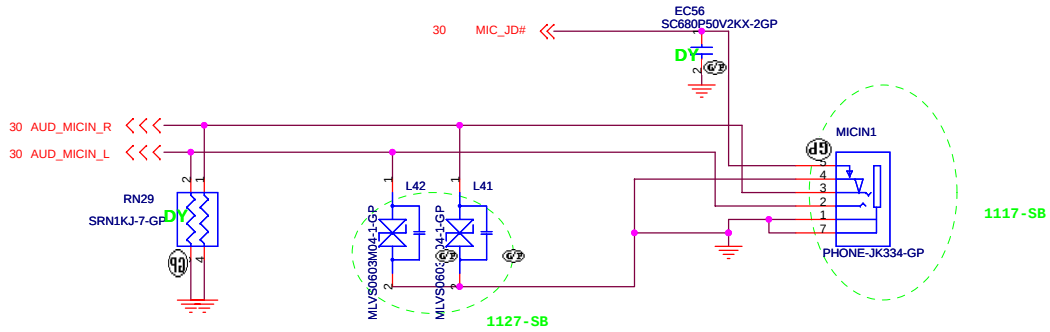
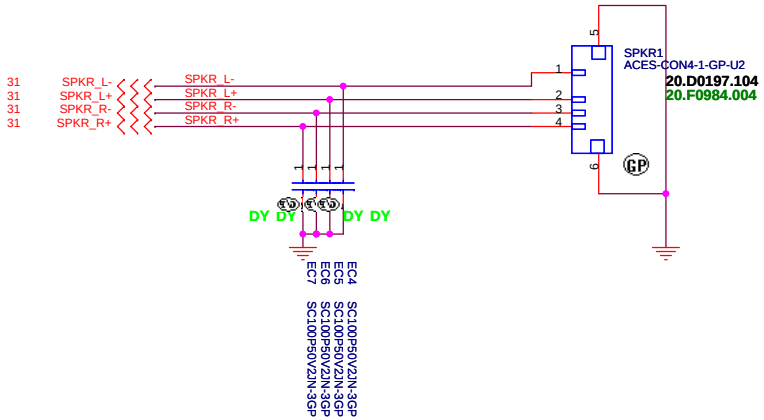
LINE OUT



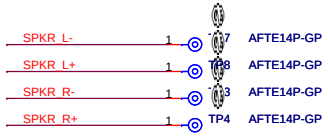
MIC IN



Internal Speaker



SPKR1 Conn. Test Point



SM30

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Title	*AUDIO JACK*	
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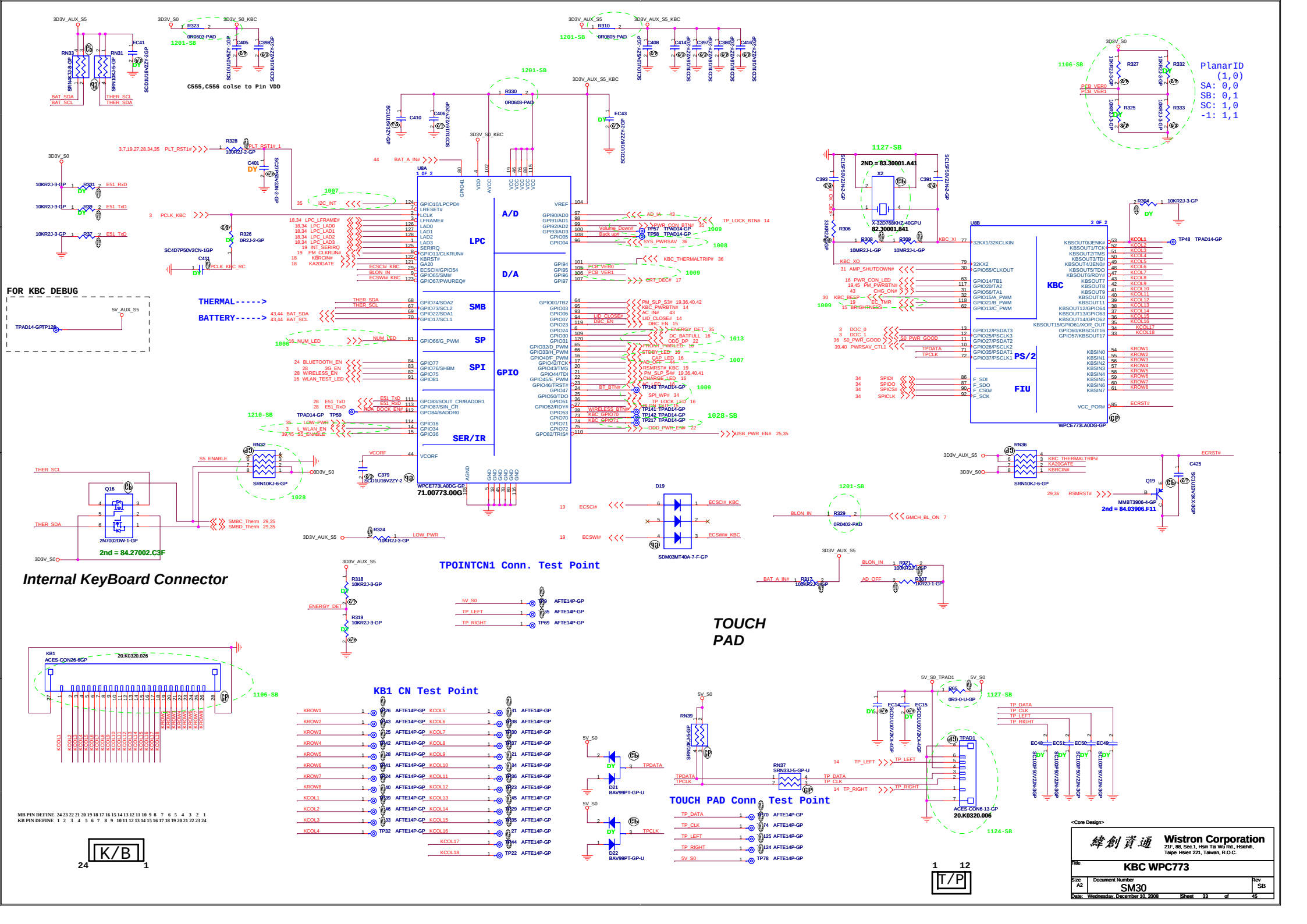
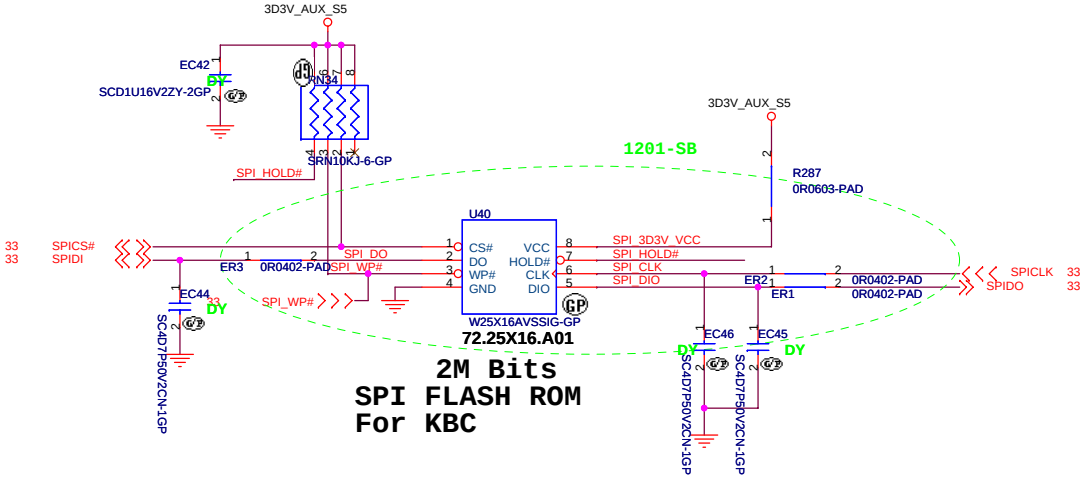
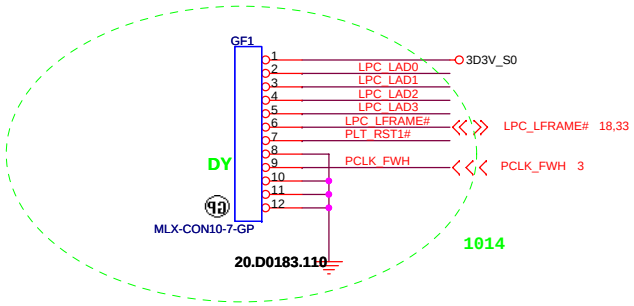
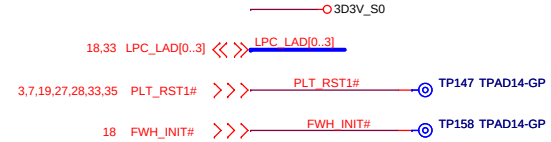
Date: Wednesday, December 10, 2008	Sheet 32 of 45	


FOR KBC DEBUG
THERMAL----->
BATTERY----->
Internal KeyBoard Connector
TOUCH PAD
TPOINTCN1 Conn. Test Point
KB1 CN Test Point
TOUCH PAD Conn. Test Point
U8A
WPCE773LA0DG-GP
71.00773.00G
U8B
WPCE773LA0DG-GP
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
2nd = 84.27002.C3F
2nd = 84.03906.F11
PlanarID (1,0)
SA: 0,0
SB: 0,1
SC: 1,0
-1: 1,1
Wistron Corporation
KBC WPC773
SM30
Wednesday, December 10, 2008





GOLDEN FINGER FOR DEBUG BOARD



TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

SM30

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Title	***BIOS & TPM***	
Size	Document Number: **SM30**	Rev: SB
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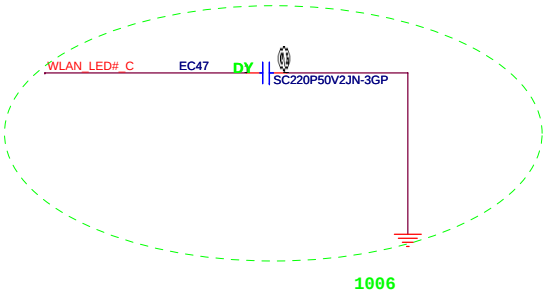
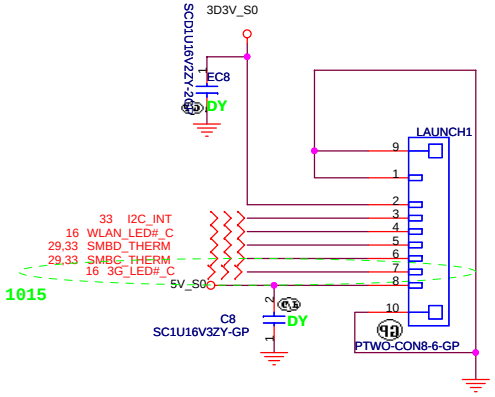
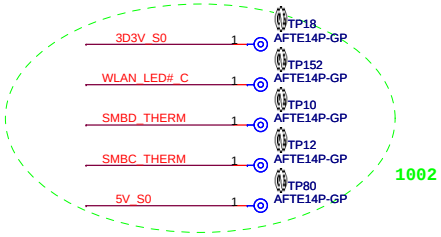
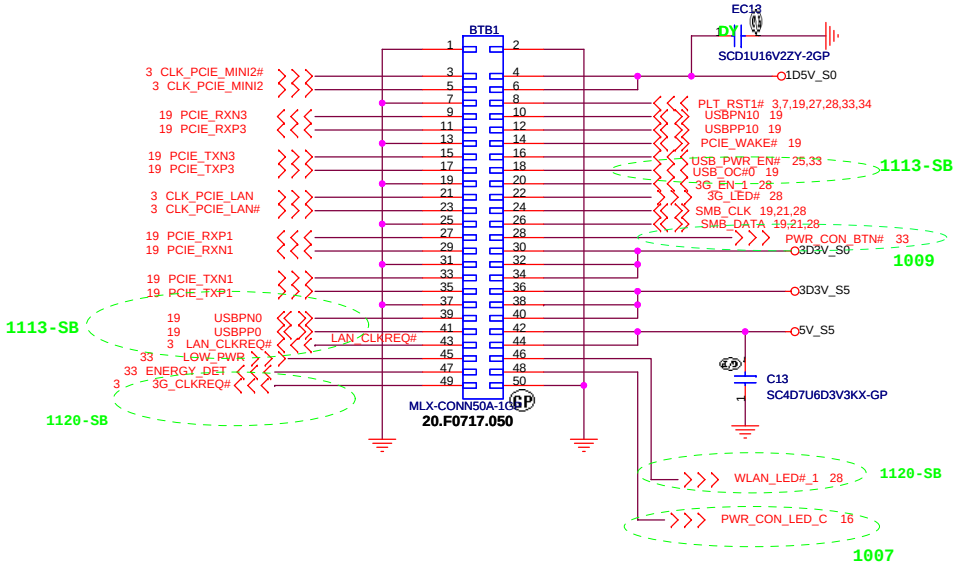
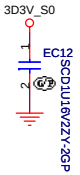


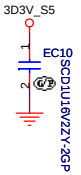


LAUNCH Test Point









SM30

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Title	LAUNCH	
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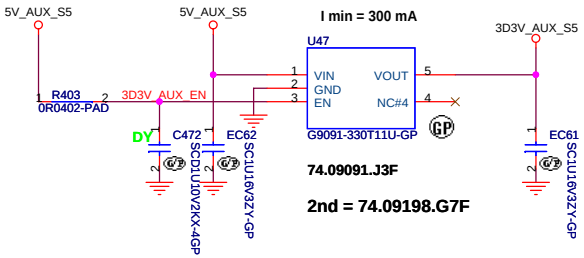
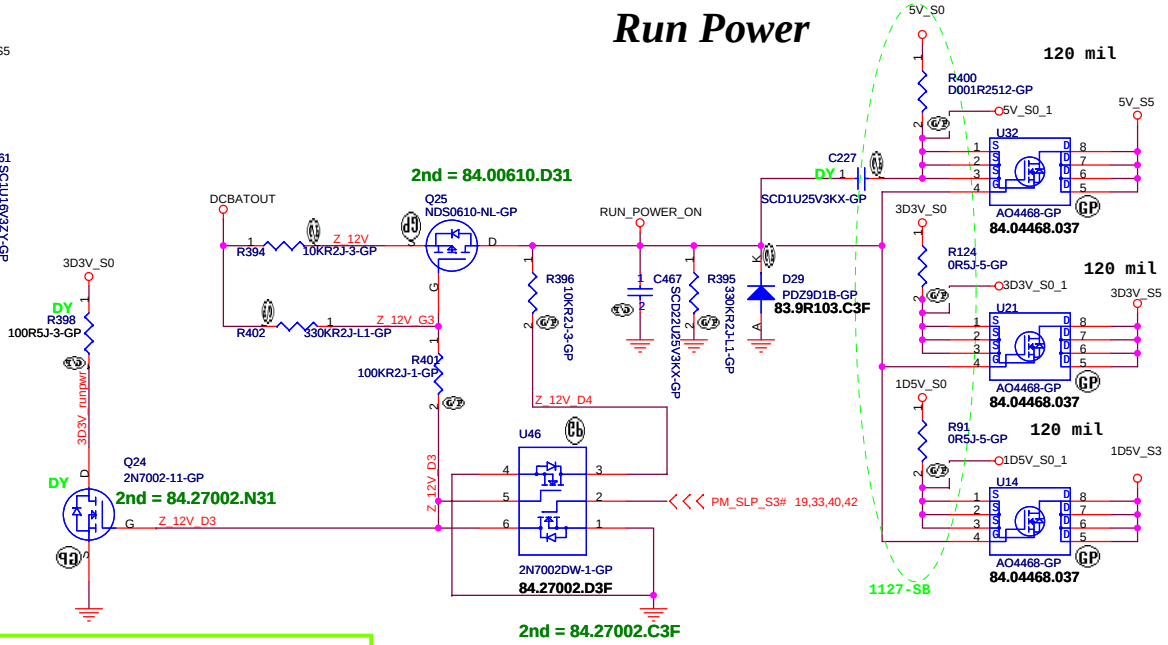
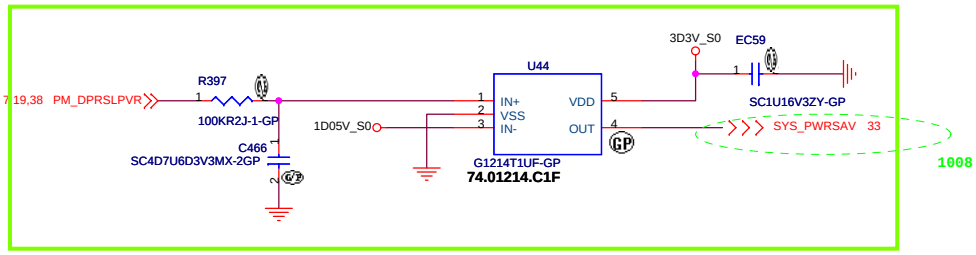
Aux Power

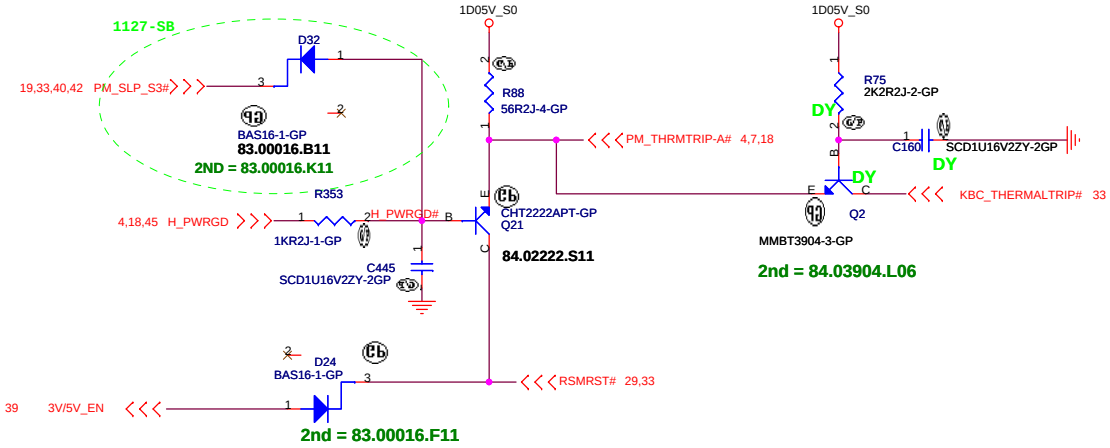
3D3V_AUX_S5

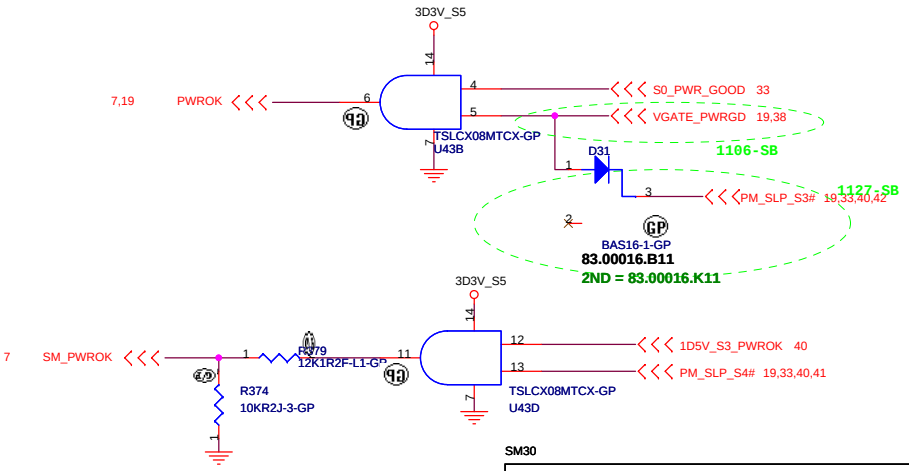


Run Power









SM30

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Title: **RUN POWER and 3D3V_AUX_S5**

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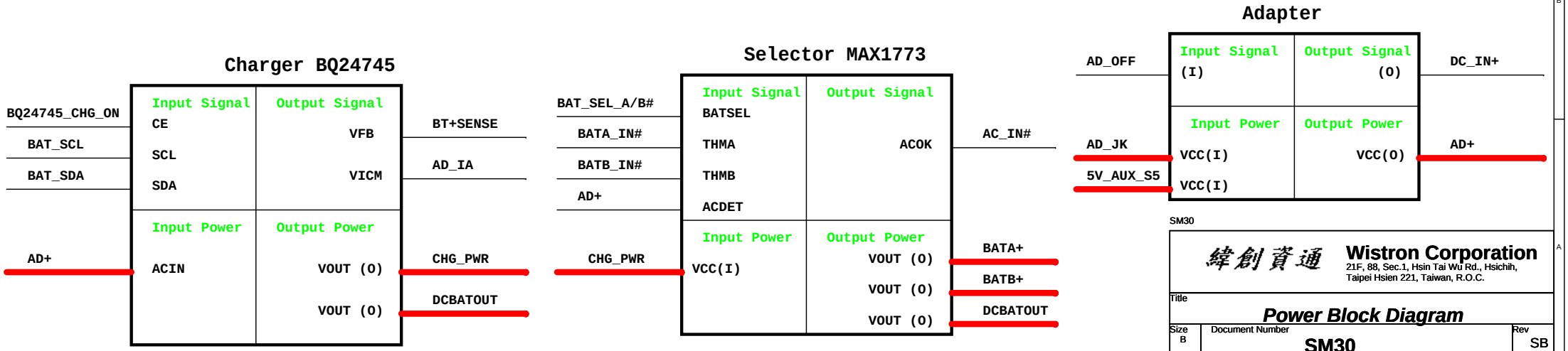
	SM30	SB

Date: Wednesday, December 10, 2008 Sheet 36 of 45



SM30

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

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B	SM30	SB

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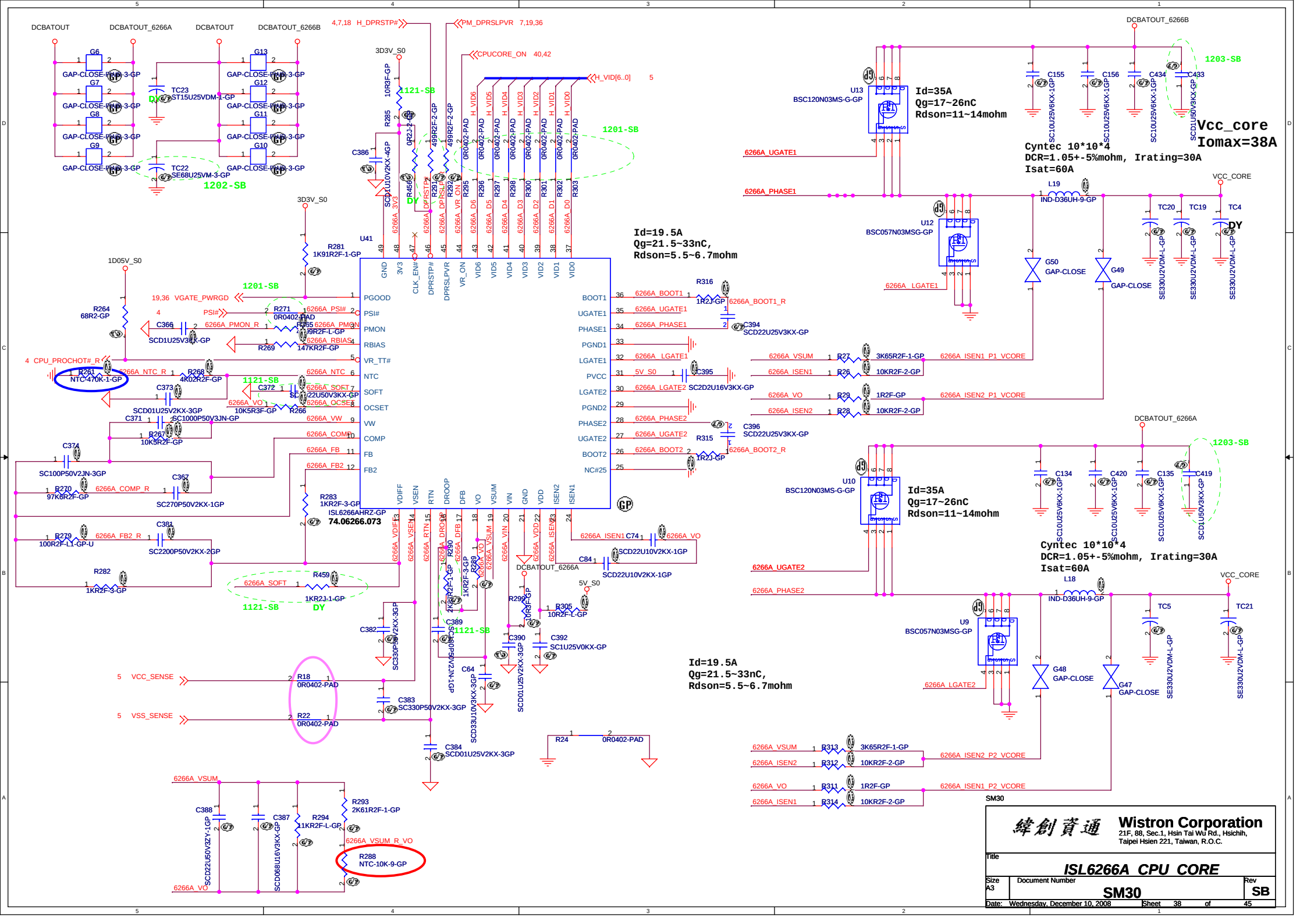
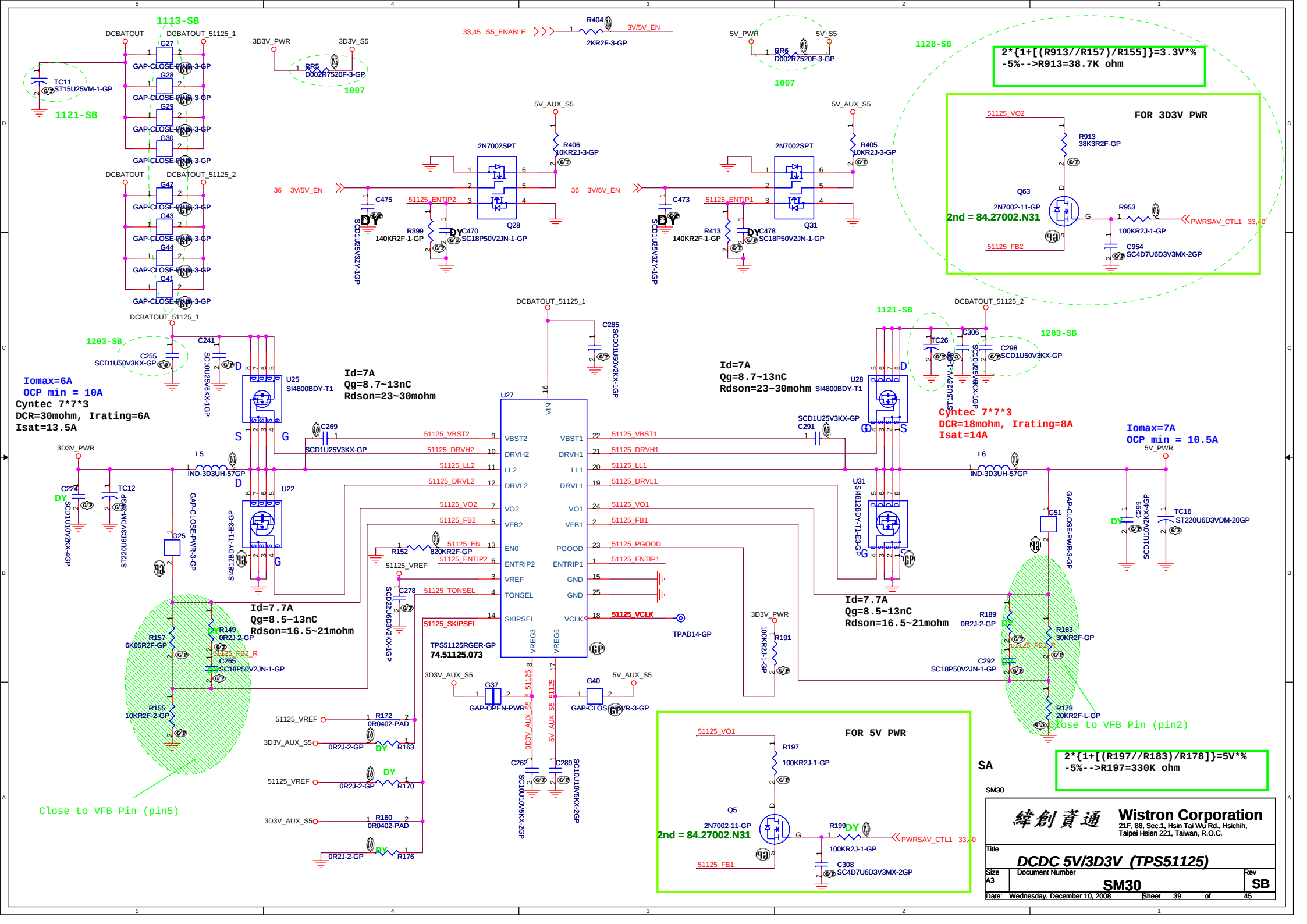

ISL6266AHRZ-GP
74.06266.073
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Vcc_core
Iomax=38A
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6266A CPU CORE
SM30
Wednesday, December 10, 2008


1113-SB
1121-SB
1007
1128-SB
1203-SB
DCBATOUT
DCBATOUT_51125_1
DCBATOUT_51125_2
3D3V_PWR
3D3V_S5
5V_PWR
5V_S5
5V_AUX_S5
33,45 S5_ENABLE
R404 2KR2F-3-GP
3V/5V_EN
RR5 D002R7520F-3-GP
RR6 D002R7520F-3-GP
2N7002SPT
R406 10KR2J-3-GP
R405 10KR2J-3-GP
C475
C473
51125_ENTIP2
51125_ENTIP1
R399 140KR2F-1-GP
R413 140KR2F-1-GP
C470 SC18P50V2JN-1-GP
C478 SC18P50V2JN-1-GP
Q28
Q31
DY
SCD1U25V2ZY-1GP
2*{1+[(R913//R157)/R155]}=3.3V*%
-5%-->R913=38.7K ohm
FOR 3D3V_PWR
51125_VO2
R913 38K3R2F-GP
Q63
2N7002-11-GP
2nd = 84.27002.N31
R953 100KR2J-1-GP
C954 SC4D7U6D3V3MX-2GP
51125_FB2
PWRSAV_CTL1 33,40
TC11 ST15U25VM-1-GP
G27 G28 G29 G30 G42 G43 G44 G41
GAP-CLOSE-PWR-3-GP
C241 SC10U25V6KX-1GP
C255 SCD1U50V3KX-GP
U25 SI4800BDY-T1
U22 SI4812BDY-T1-E3-GP
U27
U28
U31 SI4812BDY-T1-E3-GP
C269 SCD1U25V3KX-GP
C285 SCD1U50V2KX-1GP
C291 SCD1U25V3KX-GP
C306 ST15U25VM-1-GP
C298 SCD1U50V3KX-GP
TC26
L5 IND-3D3UH-57GP
L6 IND-3D3UH-57GP
C224 SCD1U10V2KX-4GP
TC12 ST220U6D3VDM-20GP
C299 SCD1U10V2KX-4GP
TC16 ST220U6D3VDM-20GP
G25 G51
GAP-CLOSE-PWR-3-GP
Iomax=6A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Cyntec 7*7*3
DCR=18mohm, Irating=8A
Isat=14A
Iomax=7A
OCP min = 10.5A
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
R152 820KR2F-GP
51125_EN
51125_VREF
C278 SCD22U6D3V2KX-1GP
51125_TONSEL
51125_SKIPSEL
TPS51125RGER-GP
74.51125.073
VBST2 VBST1 DRVH2 DRVH1 LL2 LL1 DRVL2 DRVL1 VO2 VO1 VFB2 VFB1 EN0 PGOOD ENTRIP2 ENTRIP1 VREF GND TONSEL GND SKIPSEL VCLK VIN VREG3 VREG5
51125_VBST2 51125_DRVH2 51125_LL2 51125_DRVL2 51125_VO2 51125_FB2 51125_EN 51125_PGOOD 51125_ENTIP2 51125_ENTIP1 51125_VCLK
TPAD14-GP
R157 6K65R2F-GP
R149 0R2J-2-GP
51125_FB2_R
C265 SC18P50V2JN-1-GP
R155 10KR2F-2-GP
R189 0R2J-2-GP
R183 30KR2F-GP
C292 SC18P50V2JN-1-GP
R178 20KR2F-L-GP
R191 100KR2J-1-GP
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
R172 0R0402-PAD
R163 0R2J-2-GP
R170 0R2J-2-GP
R160 0R0402-PAD
R176 0R2J-2-GP
G37 GAP-OPEN-PWR
G40 GAP-CLOSE-PWR-3-GP
C262 SC10U10V5KX-2GP
C289 SC10U10V5KX-2GP
FOR 5V_PWR
51125_VO1
R197 100KR2J-1-GP
Q5
2N7002-11-GP
2nd = 84.27002.N31
R199 100KR2J-1-GP
C308 SC4D7U6D3V3MX-2GP
51125_FB1
PWRSAV_CTL1 33,40
2*{1+[(R197//R183)/R178]}=5V*%
-5%-->R197=330K ohm
SA
SM30
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (TPS51125)
Size A3
Document Number SM30
Rev SB
Date: Wednesday, December 10, 2008
Sheet 39 of 45

Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))

0.76*{1+[(R207//R5)/R3]}=1D5V*%
-5%-->R207=210K ohm
-10%-->R207=104K ohm

SA

FOR 1D5V_PWR
1D5V_PWR
R207 210KR2F-GP
1128-SB
Q7
2N7002-11-GP
2nd = 84.27002.N31
1113-SB
R209
100KR2J-1-GP
PWRSAV_CTL1 33,39
51124_VFB1
C317
SC4D7U6D3V3MX-2GP

1D5V_PWR 1D5V_S3
RR2 D002R7520F-3-GP
1007

DCBATOUT DCBATOUT_51124_1
G52 G53 G54
GAP-CLOSE-PWR-3-GP
TC18 ST15U25VDM-1-GP
DCBATOUT DCBATOUT_51124_2
G55 G56 G57
TC17 ST15U25VM-1-GP
1121-SB
1127-SB

3D3V_S5
3D3V_S0
1201-SB
RN52 SRN10KJ-11-GP-U
5V_S5
R226 3D3R3J-L-GP
C326 SC4D7U10V5KX-1GP
C331 SC1U10V3KX-3GP

1D05V_PWR
51124_VFB2
51124_VFB1
R380 0R0402-PAD
R216 0R0402-PAD
1D5V_S3_PWROK 36
CPUCORE_ON 38,42
51124RGER_PG1
51124RGER_PG2

U35
VFB1 VFB2 VO1 VO2 PGOOD1 PGOOD2
V5FILT V5IN EN1 EN2 GND GND PGND2 PGND1 TRIP1 TRIP2 VBST1 VBST2 TONSEL
DRVH1 LL1 DRVL1 DRVH2 LL2 DRVL2
TPS51124RGER-GPU1
74.51124.073

19,33,36,41 PM_SLP_S4#
R132 0R0402-PAD
BC1 SCD47U6D3V2KX-GP
51124_V5FILT
51124_EN1
51124_EN2
19,33,36,42 PM_SLP_S3#
R219 0R0402-PAD
BC2 SCD47U6D3V2KX-GP
51124_TRIP1
51124_TRIP2
R222 20KR3F-GP
R229 20KR3F-GP
C319 SCD1U16V2KX-3GP
C320 SCD1U16V2KX-3GP
51124_LL1 R220 0R0603-PAD 51124_LL1_1
51124_LL2 R221 0R0603-PAD 51124_LL2_1
51124_VBST1
51124_VBST2
51124_TONSEL
R212 10KR2J-3-GP
R213 0R2J-2-GP
51124_V5FILT

DCBATOUT_51124_1
U4 BSC120N03MS-G-GP
84.12003.A37
U5 BSC057N03MSG-GP
84.57N03.A37
C15 SC10U25V6KX-1GP
C350 SC10U25V6KX-1GP
C14 SCD1U50V3KX-GP
1203-SB
1D5V Iomax=10A
OCP>15A
L9 IND-1D5UH-34-GP
Vout(cal)=1.5134V
R5 30K9R2F-GP
R3 30K9R2F-GP
C315 SC18P50V2JN-1-GP
C316 SCD1U10V2KX-4GP
TC1 ST330U2VDM-GP
1121-SB
Panasonic 330uF, 2V
ESR=15mohm

DCBATOUT_51124_2
U7 BSC120N03MS-G-GP
84.12003.A37
U6 BSC057N03MSG-GP
84.57N03.A37
C351 SC10U25V6KX-1GP
C24 SC10U25V6KX-1GP
C25 SCD1U50V3KX-GP
1203-SB
1D05V_PWR 1D05V_S0
RR4 D002R7520F-3-GP
1007
1D05V Iomax=10A
OCP>15A
L10 IND-D88UH-GP
R4 11KR2F-L-GP
R2 30K2R2F-GP
C5 SC18P50V2JN-1-GP
C34 SCD1U10V2KX-4GP
TC3 ST330U2VDM-GP
1204-SB
1121-SB
Panasonic 330uF, 2V
ESR=15mohm

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

SM30

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Title: TPS51124 1D5V 1D05V

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A3	SM30	SB

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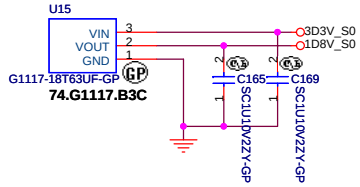

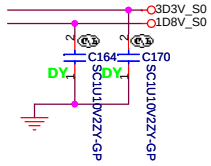

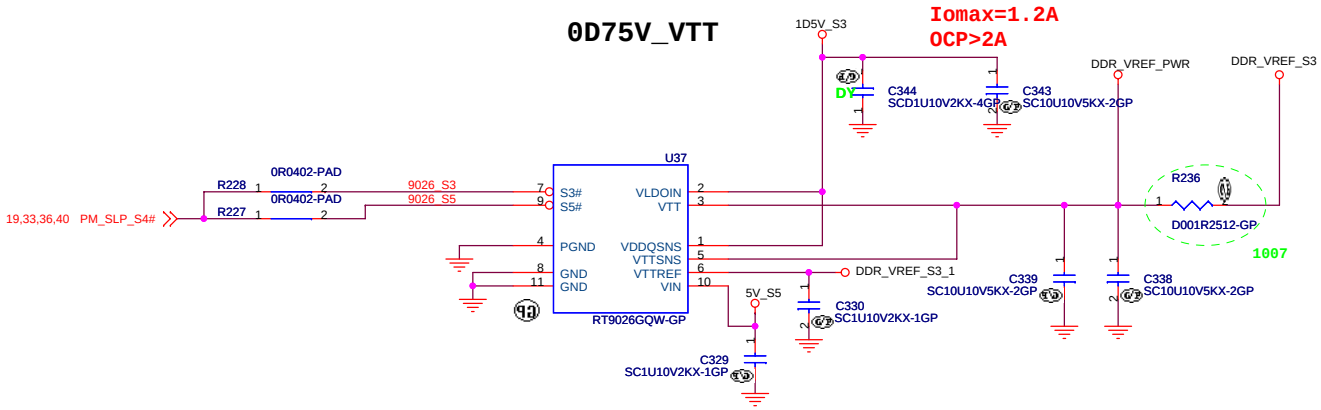

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Title	***0D75V & 1D8V***
Size A3	Document Number **SM30** Rev **SB**
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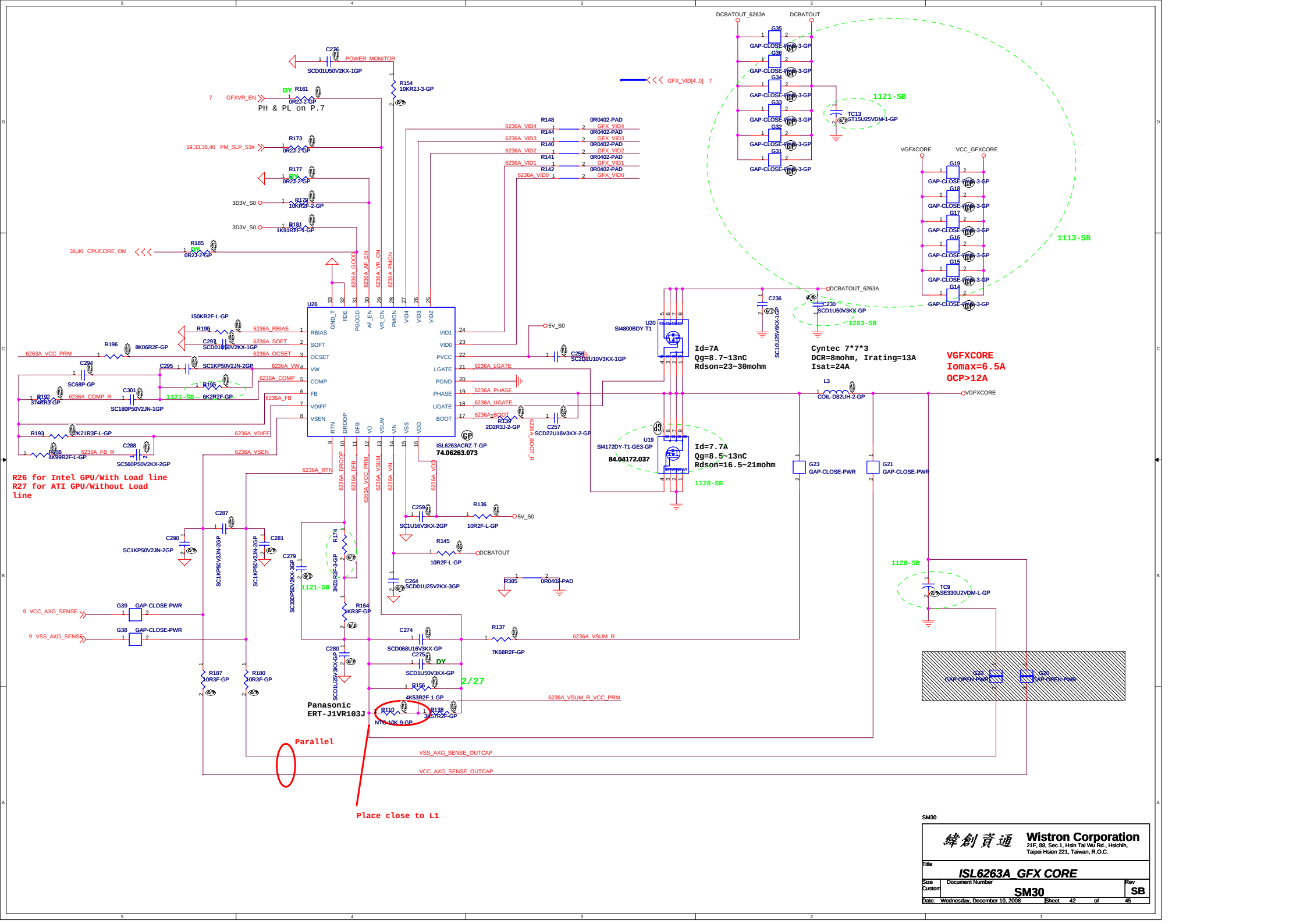
U26
ISL6263ACRZ-T-GP
74.06263.073
U19
SI4172DY-T1-GE3-GP
84.04172.037
U20
SI4800BDY-T1
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Cyntec 7*7*3
DCR=8mohm, Irating=13A
Isat=24A
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
VGFXCORE
Iomax=6.5A
OCP>12A
1121-SB
1113-SB
1203-SB
1128-SB
R26 for Intel GPU/With Load line
R27 for ATI GPU/Without Load line
Panasonic
ERT-J1VR103J
Parallel
Place close to L1
2/27
PH & PL on P.7
POWER_MONITOR
GFX_VID[4..0]
VSS_AXG_SENSE_OUTCAP
VCC_AXG_SENSE_OUTCAP
SM30
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ISL6263A_GFX CORE
Size: Custom
Document Number: SM30
Rev: SB
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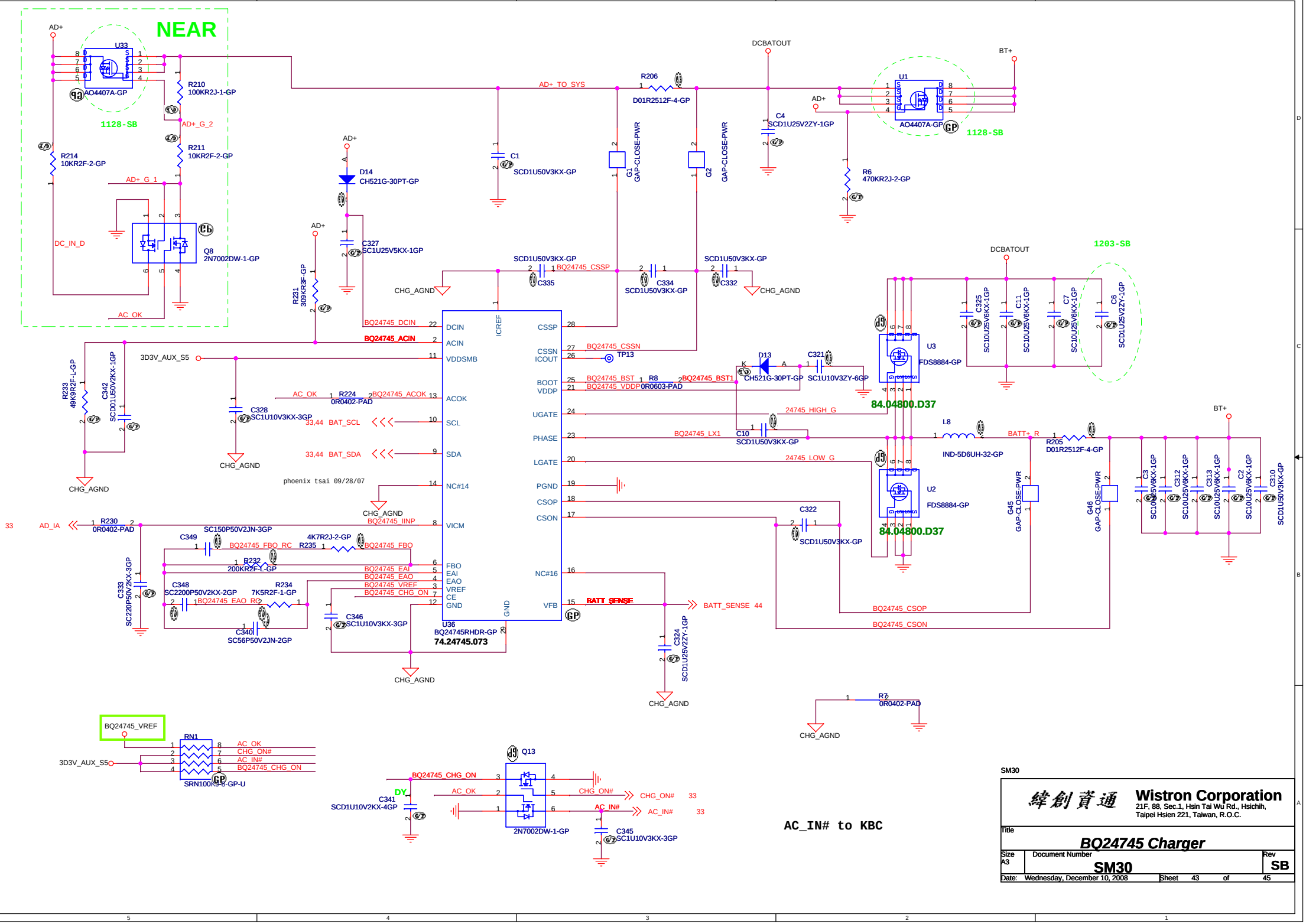

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Title	**BQ24745 Charger**	
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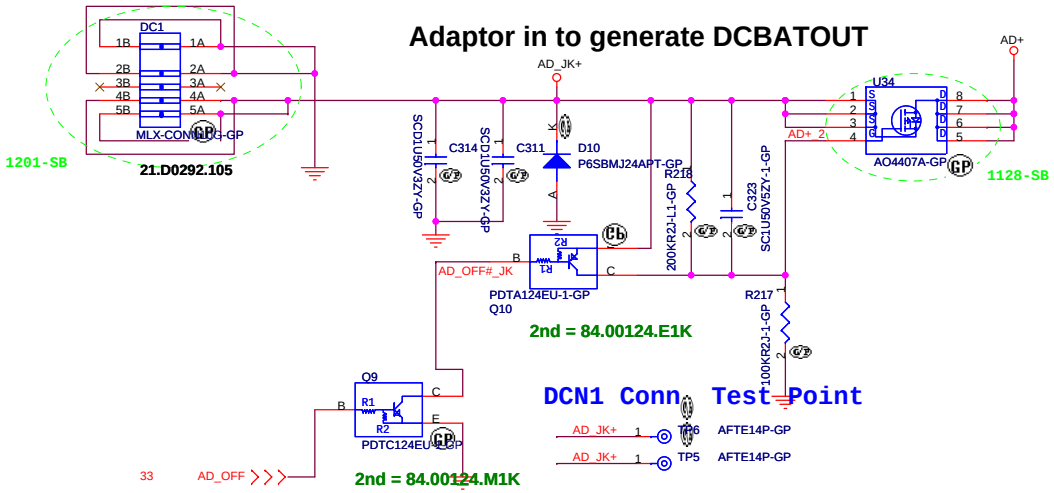
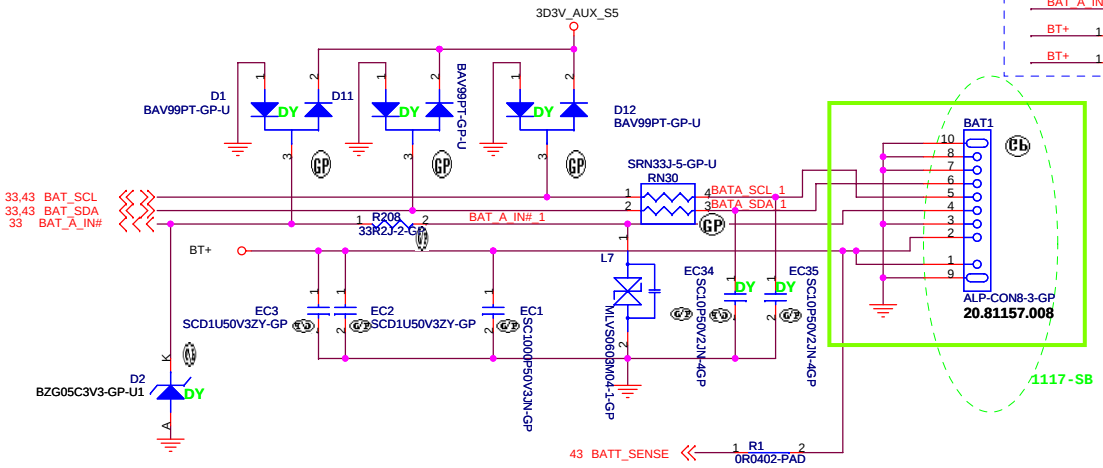
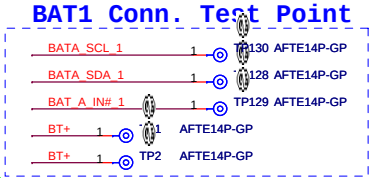
Adaptor in to generate DCBATOUT



MAIN BATTERY CONNECTOR



BAT1 Conn. Test Point



<Core Design>

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Title: **AD&BTY CONNECTER & BTY SWITCH**

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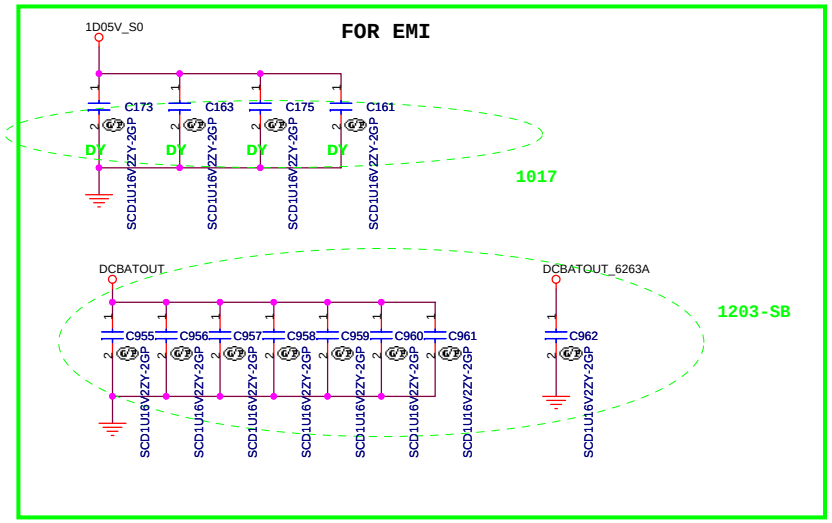
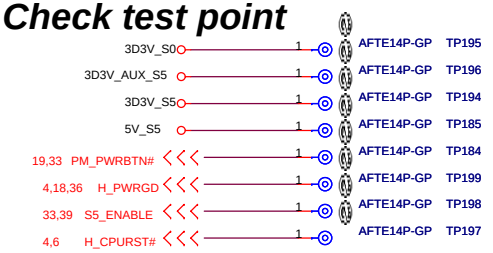
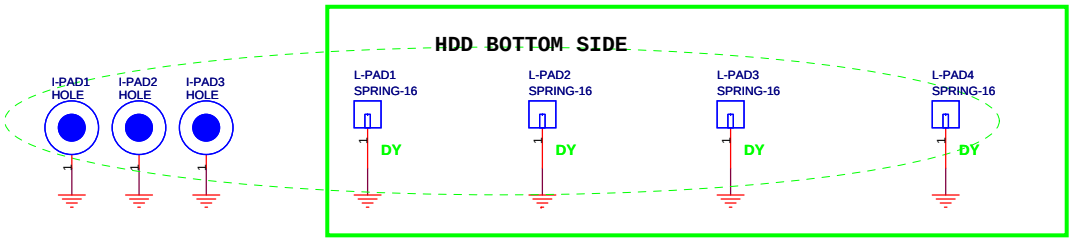
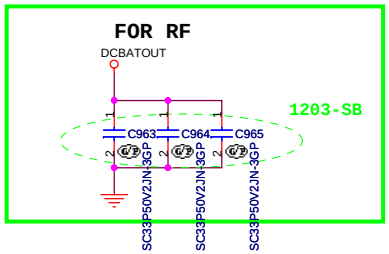


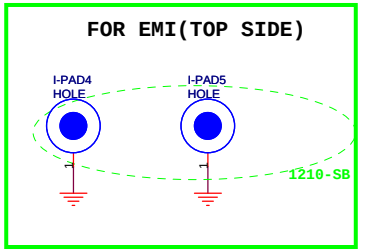
Check test point

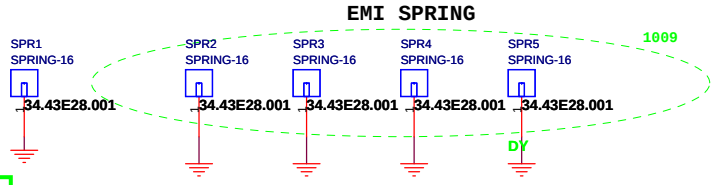


Test Point put on area where Dimm Door can be opend for measurement

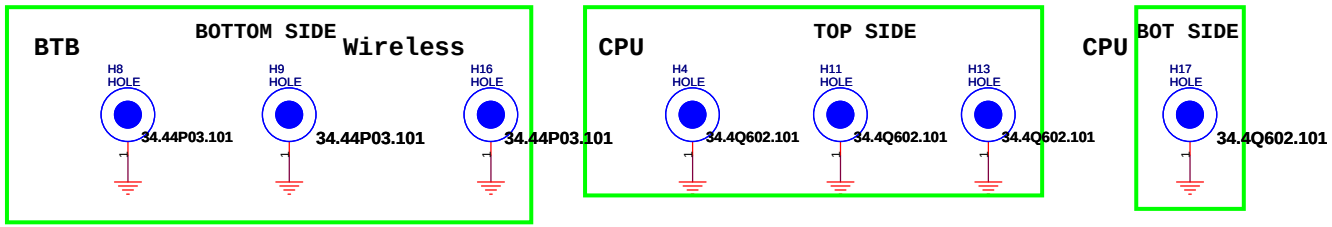








Stand off Location



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Title: ***EMI/Spring/Boss***

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